Hardware Design of a Leaky Integrate and Fire Neuron Core Towards the Design of a Low-power Neuro-inspired Spike-based Multicore SoC

Kanta Suzuki, Yuichi Okuyama, Abderazek Ben Abdallah
School of Computer Science and Engineering
Adaptive Systems Laboratory
The University of Aizu, Japan

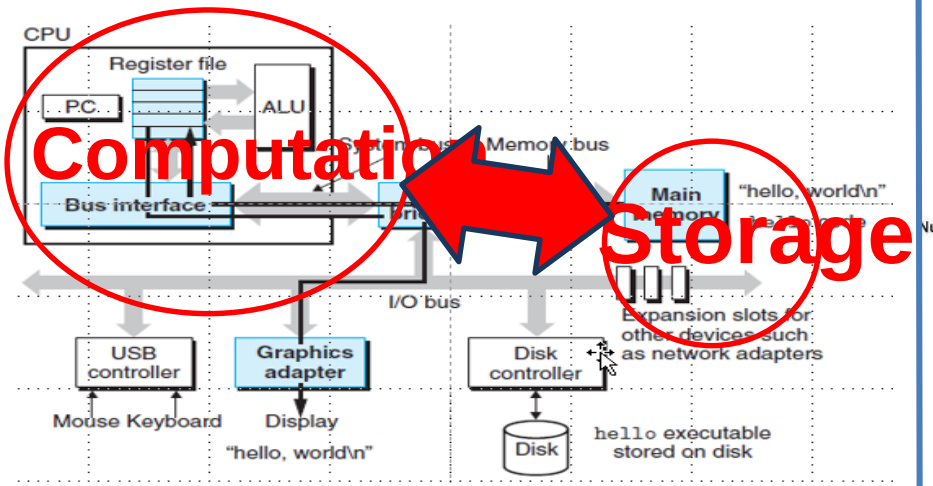
Outline

- Background
- NASH Architecture Overview
- Research Contribution
- Neuro-core Architecture
- Design & Evaluation Result
- Conclusion and Future Work

Background

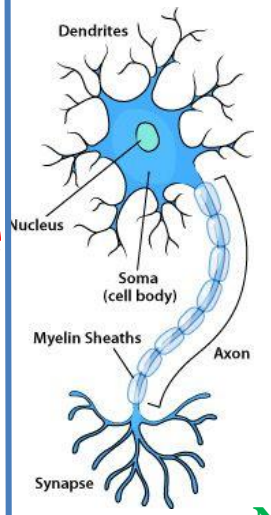
- The architecture of conventional computer systems is very different from the organization of the brain.
- Silicon circuits generally use a global clock to coordinate activities while the brain operates in an asynchronous manner.
- Memory and computation circuits in conventional computers are separated, while memory and computation appear to be tightly integrated in brains.
- The fan-out of a CMOS element is small relative to the thousands of connections made by an individual neuron to others.

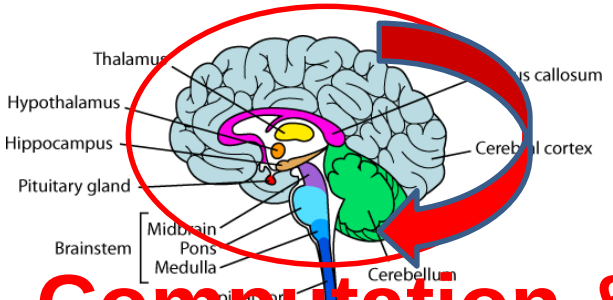
Ld/St vs. Neuro-inspired Computing



Load-Store Computing

- High Power
- Storage and computation are separated
- Poor at recognition

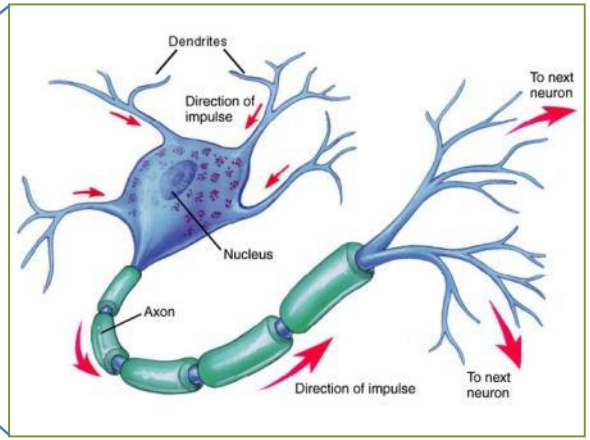


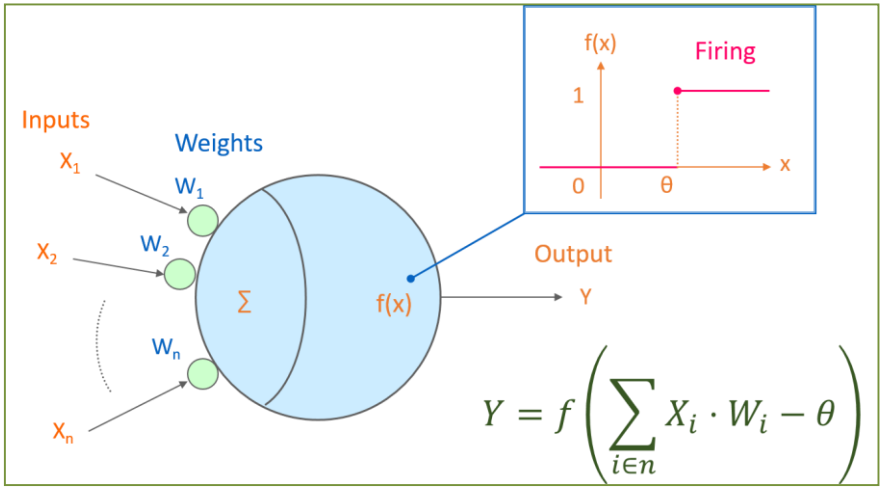


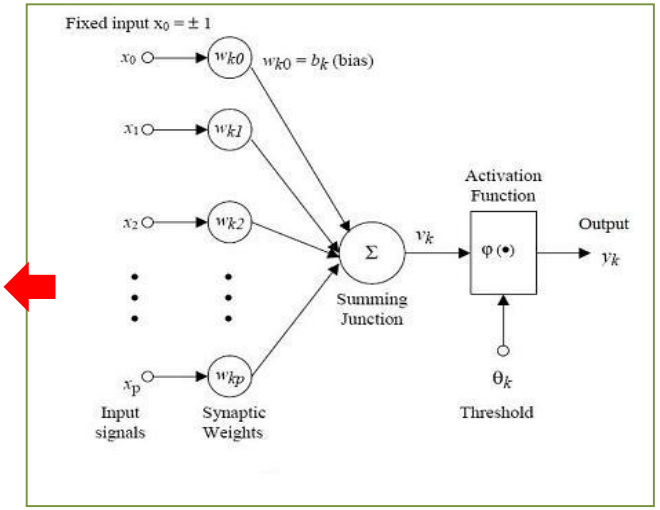
Neuro/Brain-inspired Computing

- Low Power
- Storage and computation are not separated
- Good at recognition

Simple Neuron Organization







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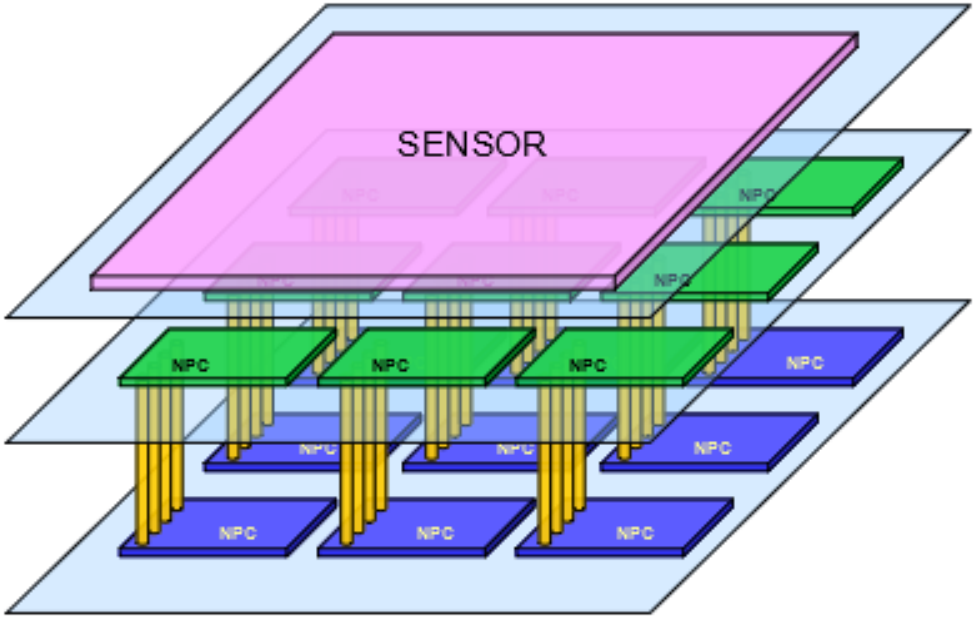
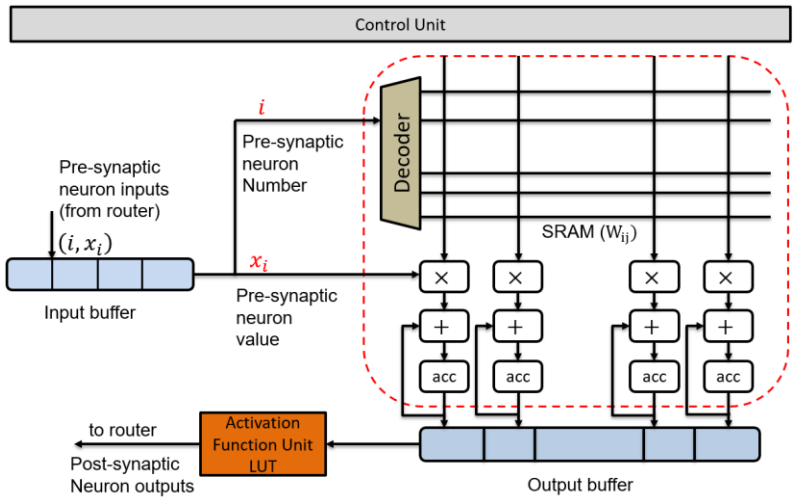
Neuro-inspired ArchitectureS in Hardware - NASH



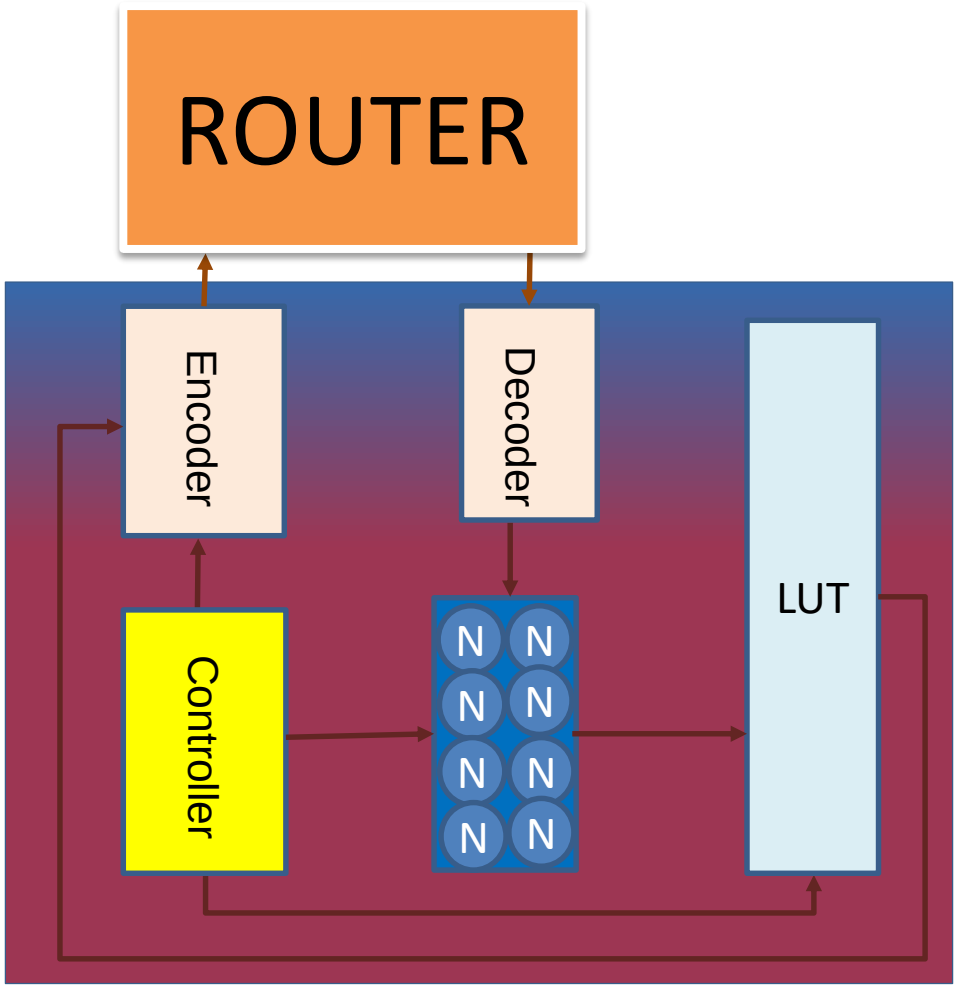


SRAM based Neuro Processing Core (NPC)

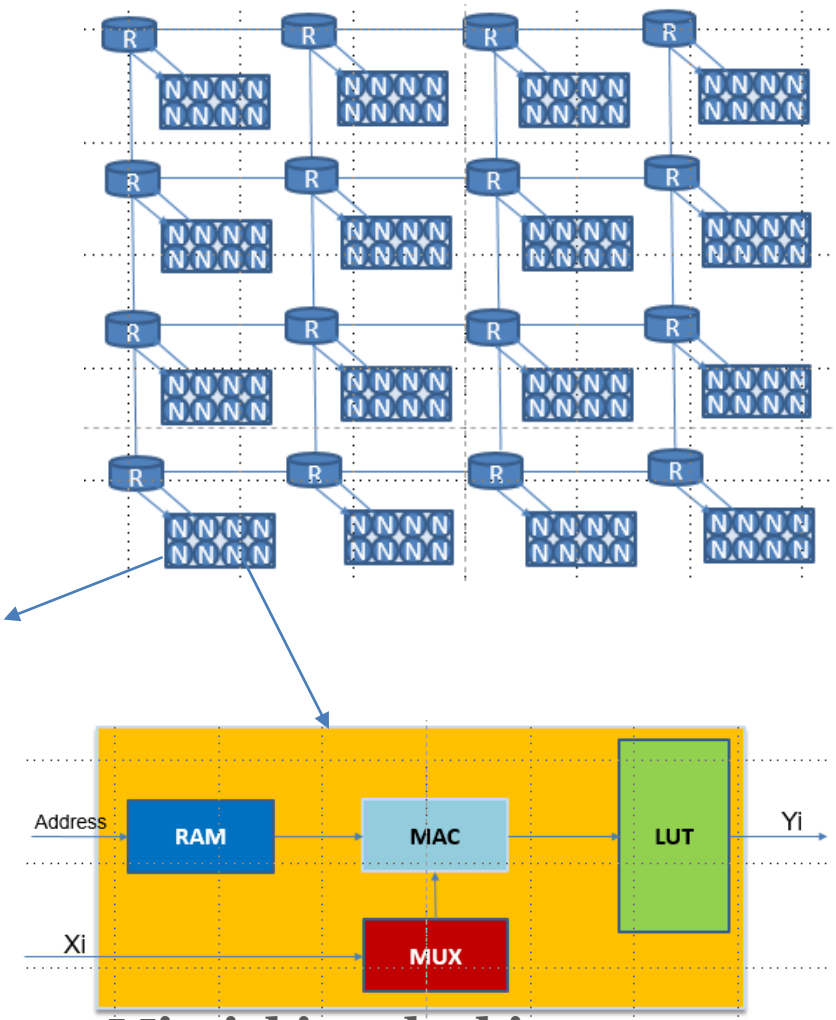
- NASH processes data directly coming from sensors via 3d-TSV → no need to go from sensors to memory and back to the processor.
- High throughput applications require more off-chip (~20Gbps) bandwidth.

- Each core processes a collection of N neurons each with M synaptic weights Wij.
- 8-bits are used to store the synaptic weights in SRAM.
- Every neuron input and output are also 8-bit wide.

Neuro-inspired ArchitectureS in Hardware - NASH

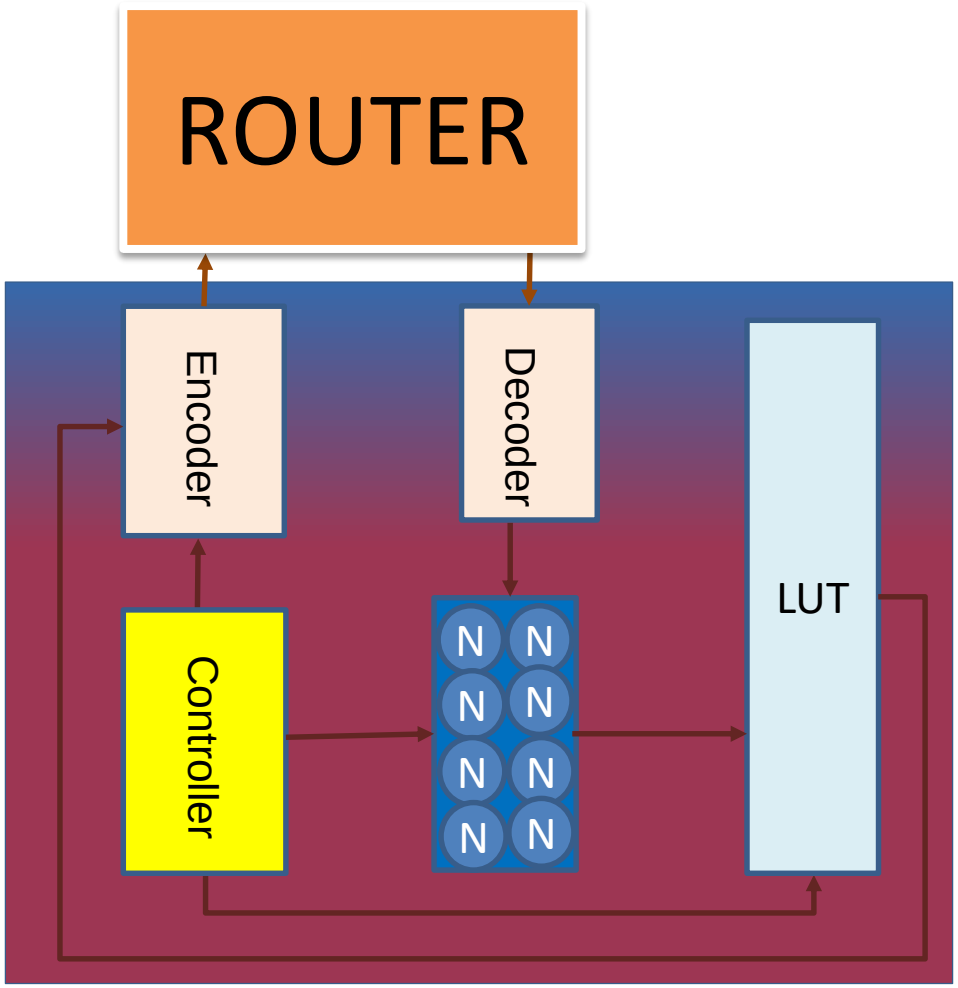


Structure of one PE



Mimicking the bio-neuron

Neuro-inspired ArchitectureS in Hardware - NASH



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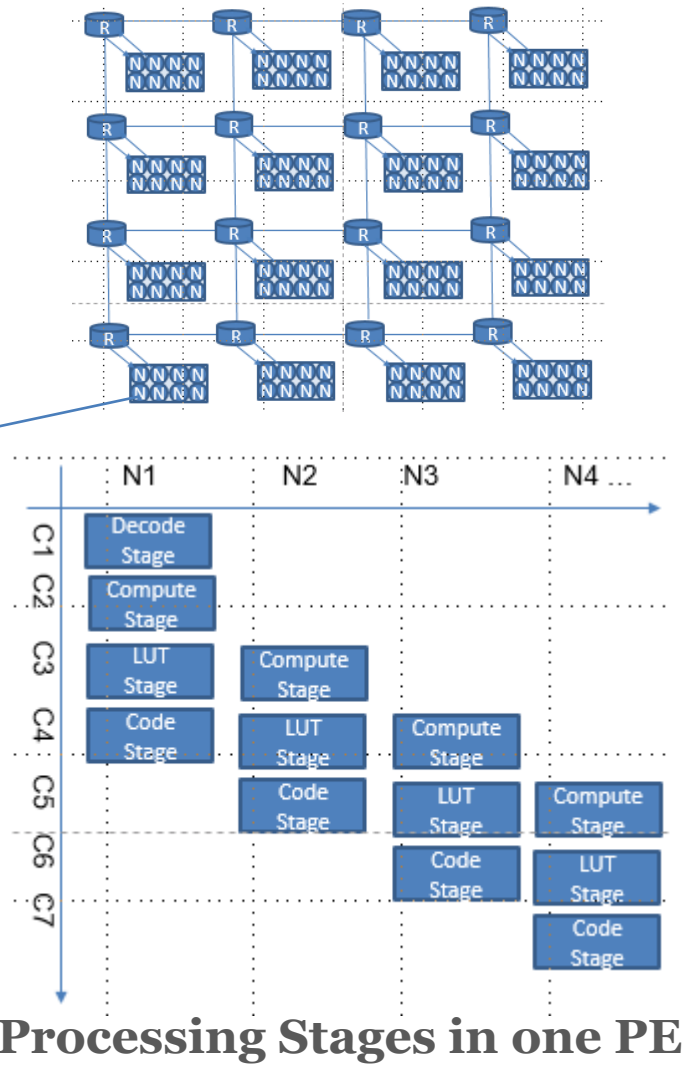

Processing Stages in one PE

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Research Contribution

- This work presents a hardware design of a Leaky Integrate and Fire Neuron-Core to be integrated with a a Low-power Neuro-inspired Spike-based Multicore SoC

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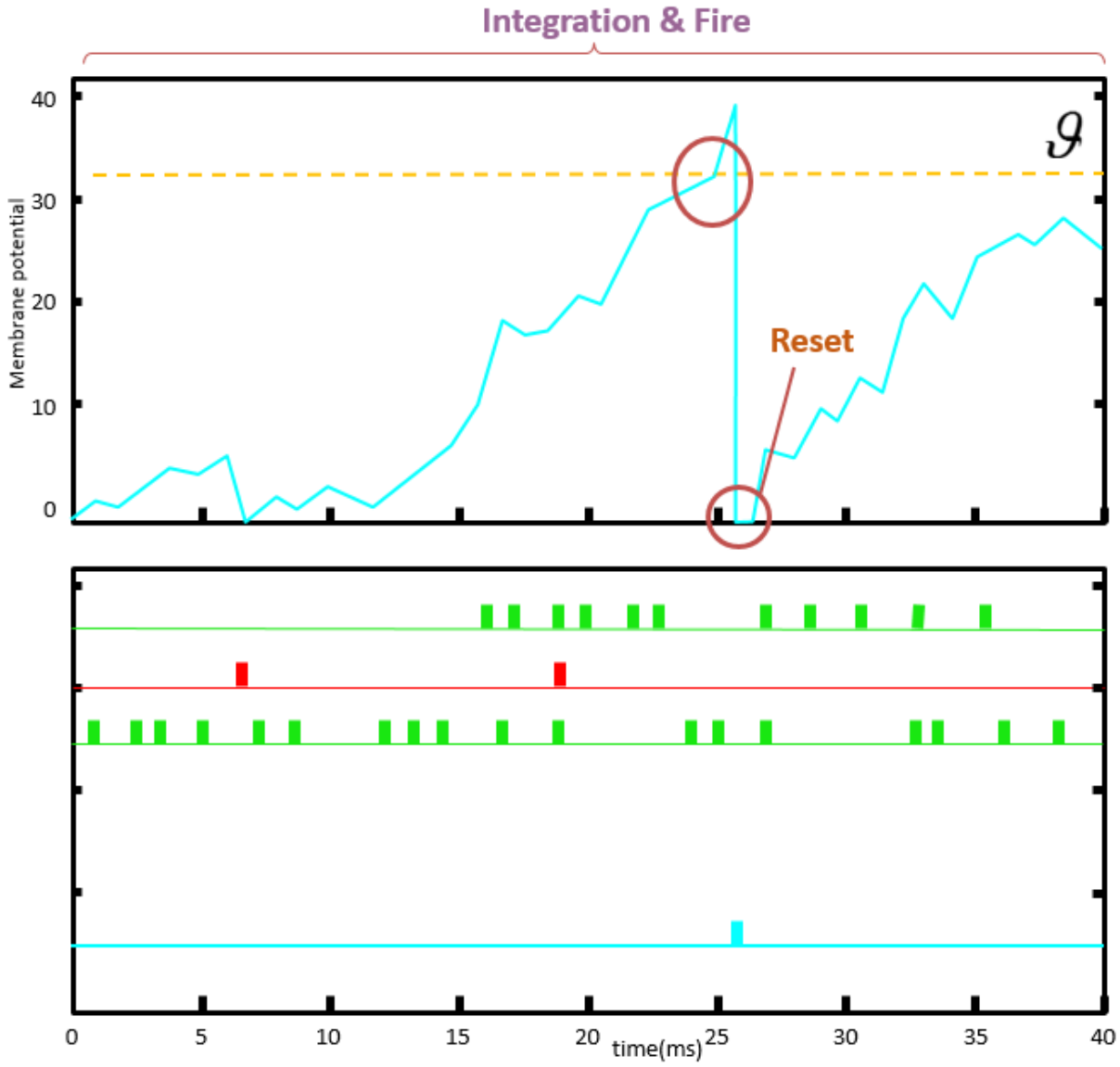
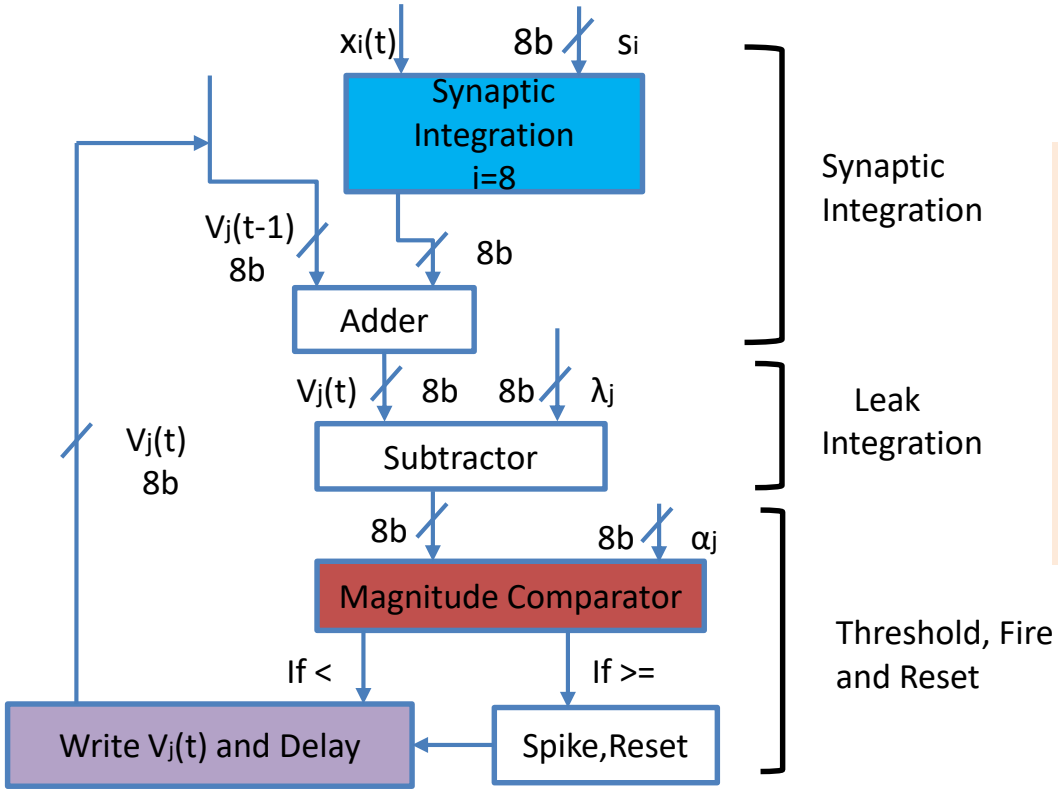
Leaky Integrate and Fire Spiking Neuron Model



Neuro-core Architecture

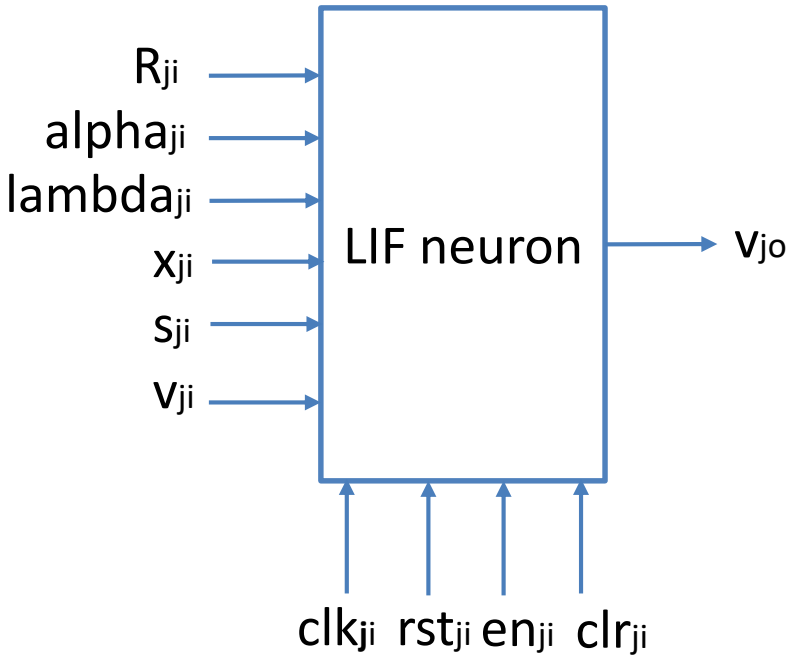


- Xi(t) – Spike input to the synapse
- Si – synaptic weight
- Vj(t) – Membrane potential
- αj – Neuron threshold
- Λj – Leak value

Hardware structure and flow of LIF neuron

Neuro-core Architecture

Architecture visualization



- Membrane potential – signed integer 8bits (-128,127)
- Spike input - 1bit (0,1)
- Spike output – 1bit (0,1)
- Synaptic weights – signed integer 8bits (-128,127)
- Neuron threshold – signed integer 8bits (-128,127)
- Leak value – unsigned integer 8bits (0,255)

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Design & Evaluation Methodology

- The Neuro-core was designed in Verilog HDL
- Synthesis with Quartus II and Cadence
- Evaluation of:
  - Correctness
  - Power
  - Frequency
  - Area

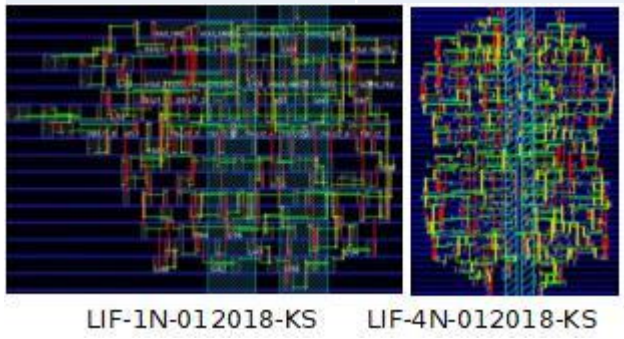
Hardware Design Result

Table 1: Area Evaluation

Item	NC-1N	NC-4N
Combinational Area	186.998000 µm	562.856001 µm
Noncombinational Area	47.88002 µm	213.864000 µm
Total Cell Area	234.878002 µm	776.720001 µm

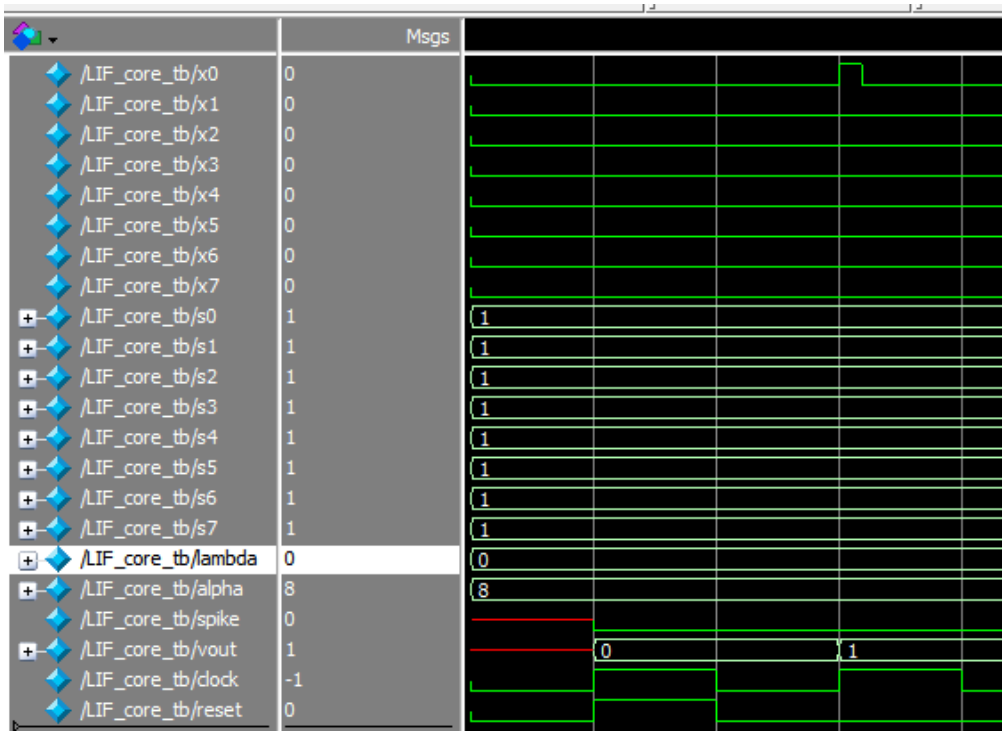
Table 3: Power Consumption Evaluation

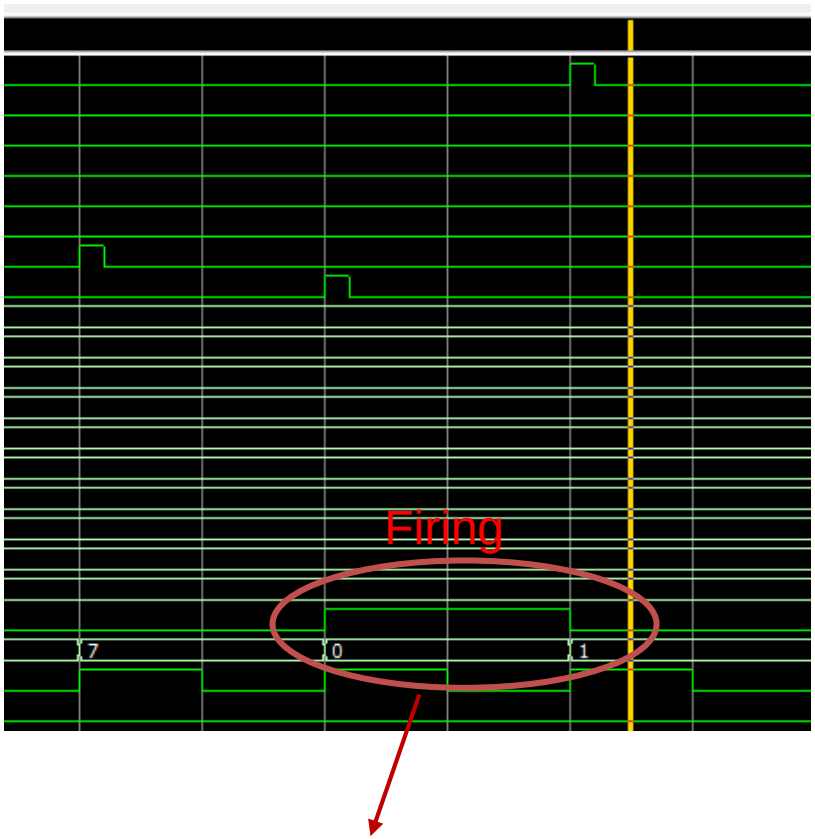
Item	NC-1N	NC-4N
Cell Internal Power	6.9680 µW	20.5040 µW
Net Switching Power	4.8271 µW	14.8272 µW
Total Dynamic Power	11.7950 µW	35.3312 µW
Cell Leakage Power	4.6943 µW	14.3147 µW



Placement of LIF-1N (Left) and LIF-4N (right)

Hardware Design Result





This case each synapsys weights is 1.
Threshold value is 8.

If membrane potential >= threshold
Firing!

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Conclusion and Future Work

- This work presents a hardware design and evaluation of a LIF Neuron-Core to be integrated with a Low-power Neuro-inspired Spike-based Multicore SoC (NASH)
- For accurate hardware complexity, the Neuro-core was designed and evaluated in hardware with several CAD tools.
- Evaluation results show that the designed Neuro-core (1 neuron) consumes about 155.36 mW and 169.32 mW (4 neurons), which is acceptable.

Conclusion and Future Work

- In future work, we intend to integrate the LIF core in our NASH system and evaluate its real performance with a real application, such as image recognition.

Thank you for your attention.