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OASIS-NP

Abderazek Ben Abdallah
Adaptive Systems Laboratory

Abstract

The biological brain implements massively parallel computations using a complex architecture that is different from current Von Neumann machine. The brain is a low-power, fault-tolerant and high-performance machine! It consumes only about 20W and brain circuits continue to operate as the organism needs even when the circuit (neuron, neuroglia, etc.) is perturbed or died. Our goal in this project is to research and develop in hardware an adaptive low-power and reliable neuro-inspired manycore SoC with on-chip learning and cognitive capabilities targeted for pattern recognition and complex cognitive tasks. Our other goal is to investigate and develop a low-power and low-cost platform for running large-scale simulations of biological brains in real-time targeted for neuroscience applications. Currently, we are investigating the following problems: the communication network for neuro-inspired chips, reconfigurability and adaptability methods, fault-tolerance, and learning circuits. In addition to these two target applications, lessons learned from this project will also be used to optimize power & performance of the conventional architectures.

Introduction

Current neural processing methods are based on so-called spiking neural networks (SNNs), which differ from conventional artificial NN models. In conventional SNNs information is transmitted using spikes or pulses (see Fig. 1). Brain-inspired models such as SNNs offer the opportunity to design a robust architecture for performing computation with low power. In particular, SNNs offer the potential to mimic the ability of the brain to tolerate faults and repair itself [1]. The brain often replaces neurons by reconnecting to newly generated neurons via synaptic junctions. This adaptability allows the brain to overcome faults.

Software simulations of traditional SNN networks face the problem of scalability in that biological computing systems are inherently parallel in their architecture whereas conventional systems are based on sequential processing architectures.

Hardware SNNs have the advantage of computational speed over software simulations and can take full advantage of their inherent parallelism. In particular, hardware SNNs can respond to the demands of real-time and fault-tolerant applications. However, the current problem of interneuron connectivity is prohibiting the implementation of these SNNs in hardware. This connectivity challenge more challenging when neuro-glia networks are considered.

One promising approach to this challenge is the use of Network-on-Chip (NoC) to support the fast exchange of information within an SNN. NoC uses packet to exchange information between different processing elements within a system.

Our goal is to develop dedicated mixed signals programmable Neural-Network architecture which will support the implementation of large-scale SNN applications.

Current FPGAs do not provide sufficient dedicated programmable hardware resources (i.e. synaptic junctions, inline training support) which needed for efficient SNN implementations. Also, FPGAs routing structures cannot accommodate the high levels of interconnection found in SNNs.

The proposed OSIS-NP architecture avoids these problems by making use of small-scale low-powered analog spiking neuron cells as the central PE. Combining small size low power neuron cells with the OASIS-NoC routing capability will lead to OASIS-NP system that can significantly increase the processing power of SNNs towards the biological scale. However, the use of the OASIS-NoC as an interconnection fabric for large scale neuro-glia networks demands a more challenging trade-off between power consumption, throughput and network scalability, and therefore an improved solution is required. Scaling is one of the key issues associated with all complex electronic systems because interconnect consumes large areas of chip real-estate and subsequently causes longer critical path delays [1].

To solve the large scale implementation issues of reconfigurability and programmability, lightweight synapse weight storage and interneuron connectivity, a new efficient architecture is required.

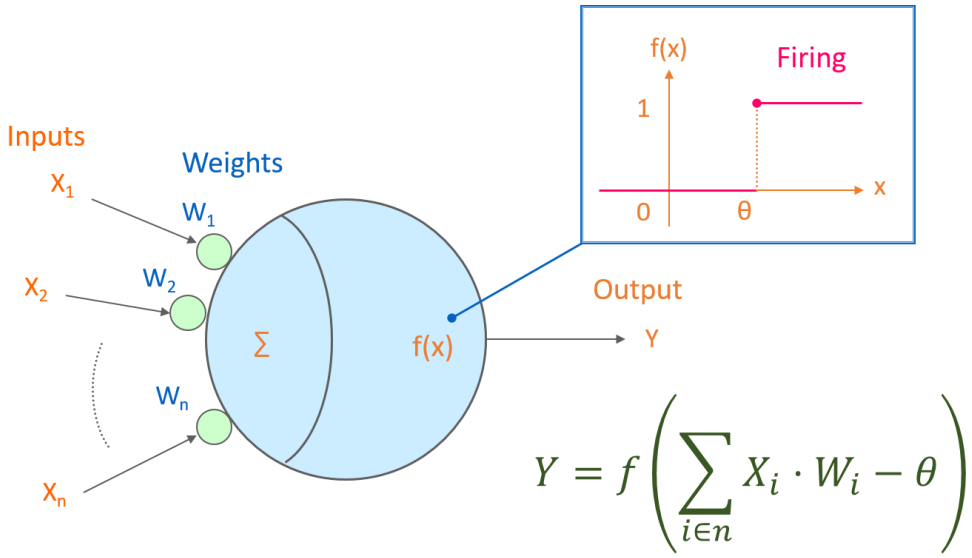
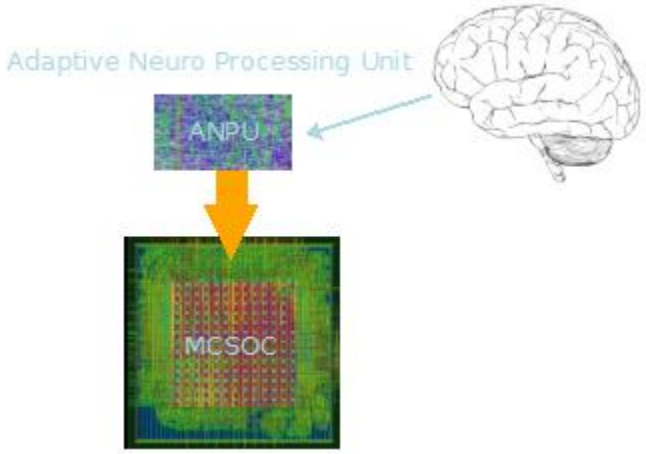


Figure 1. Neuron Model (McCulloch-Pitts Model of Neuron)

To demonstrate the OASIS-NoC implementation of an SNN, an FPGA hardware implementation will be developed and interfaced to a drone or a robot. This project is based on an existing scalable OASIS-NoC routers developed at ASL [2-21] and explored the following issues in the development of a new NoC strategy for SNN:
(1) An efficient topology and configurations which enable reconfiguration of different NoC networks in hardware;
(2) A mixture of different basic NoC topologies (OASIS-2D, OASIS-3D, etc.) will be investigated;
(3) Performance evaluation and comparisons against existing systems.



OASIS-NP High-Level View

Hardware SNN Architectures

A major challenge in developing SNNs in hardware is the development of neuro-inspired platforms which can support scalable low-power realizations and reprogrammable interconnect. In particular, the problem of interneuron connectivity is the major problem that prohibits the implementation of such SNNs.

Current attempts to realize SNNs using multiprocessors in hardware have included limited numbers of neurons due to connectivity issues [22-27].
Several full-custom neuromorphic architecture devices have been proposed [28-30] which aim to address the inefficiencies of FPGAs by including optimized synaptic cells and Address Event Representation (AER) routing [33]. However, these systems are not reconfigurable and cannot scale due to limited connectivity provided by AER between neurons.

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