

How to use High-level synthesis

What's High level synthesis?

- Convert software language to HDL
- VIVADO HLS offers platform that users can use C for FPGA implementation

What's FPGA

- Field Programmable Gate Array
 - Users can reconfigure logic circuit by programming behavior
- Users can make any hardware as they like

Brief outline

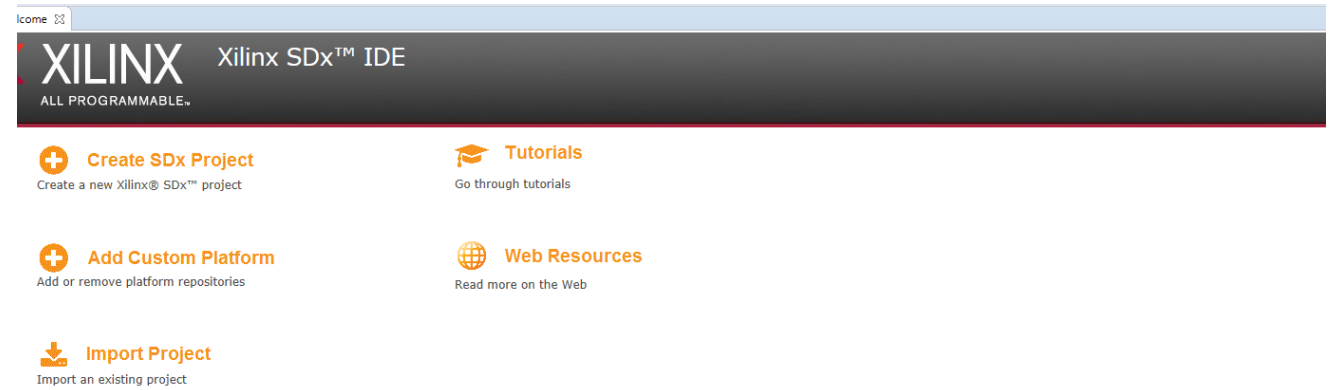
- Try high-level synthesise by using VIVADO HLS
 - Write Deep Learning code
 - Synthesize code and make bitstream file
 - Implement on FPGA

1. Run software

- Prepare FPGA “ZedBoard”
- Install “SDx IDE 2018.1”
- Run “SDx IDE 2018.1”

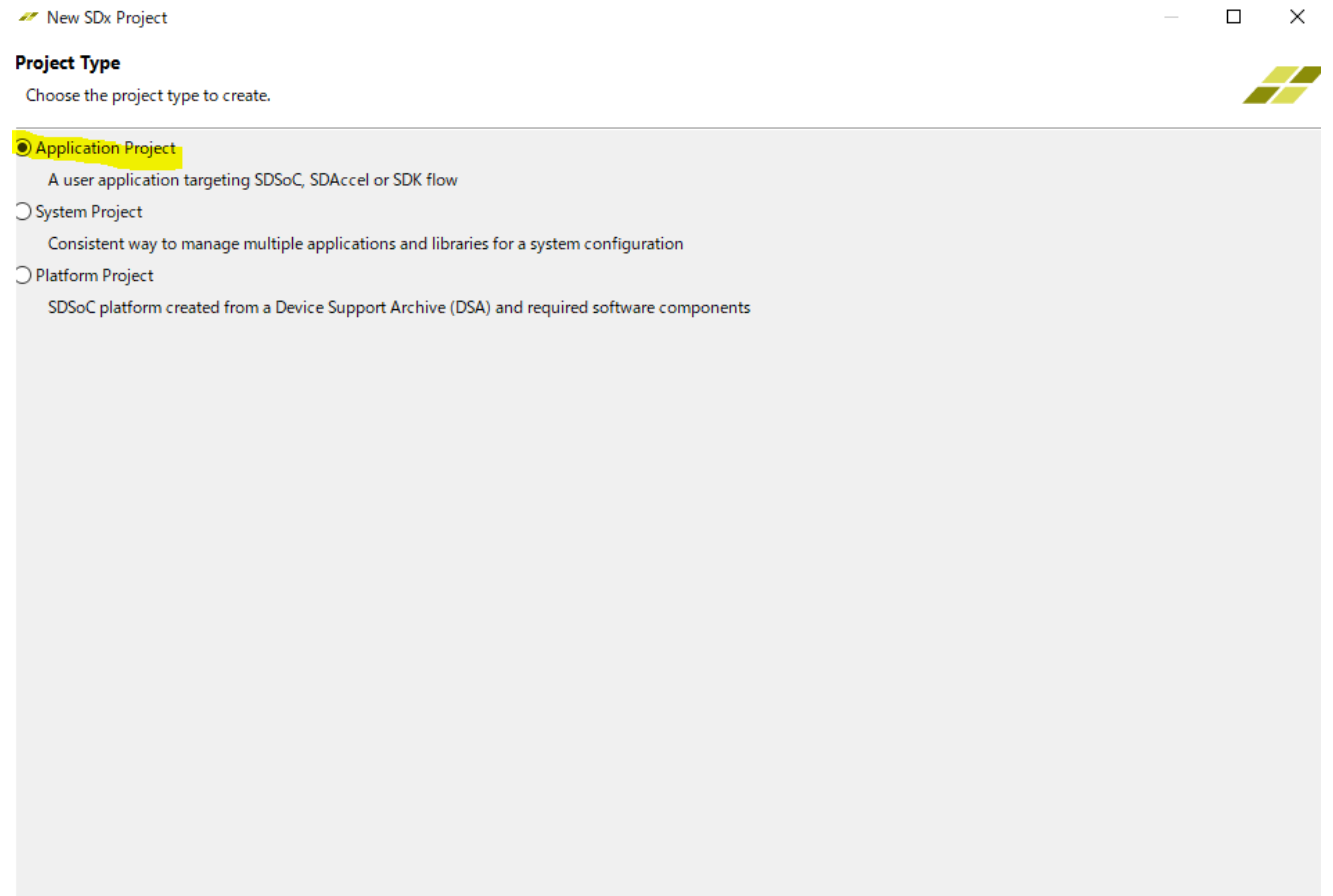
Create SDx Project

- Select “Create SDx Project”



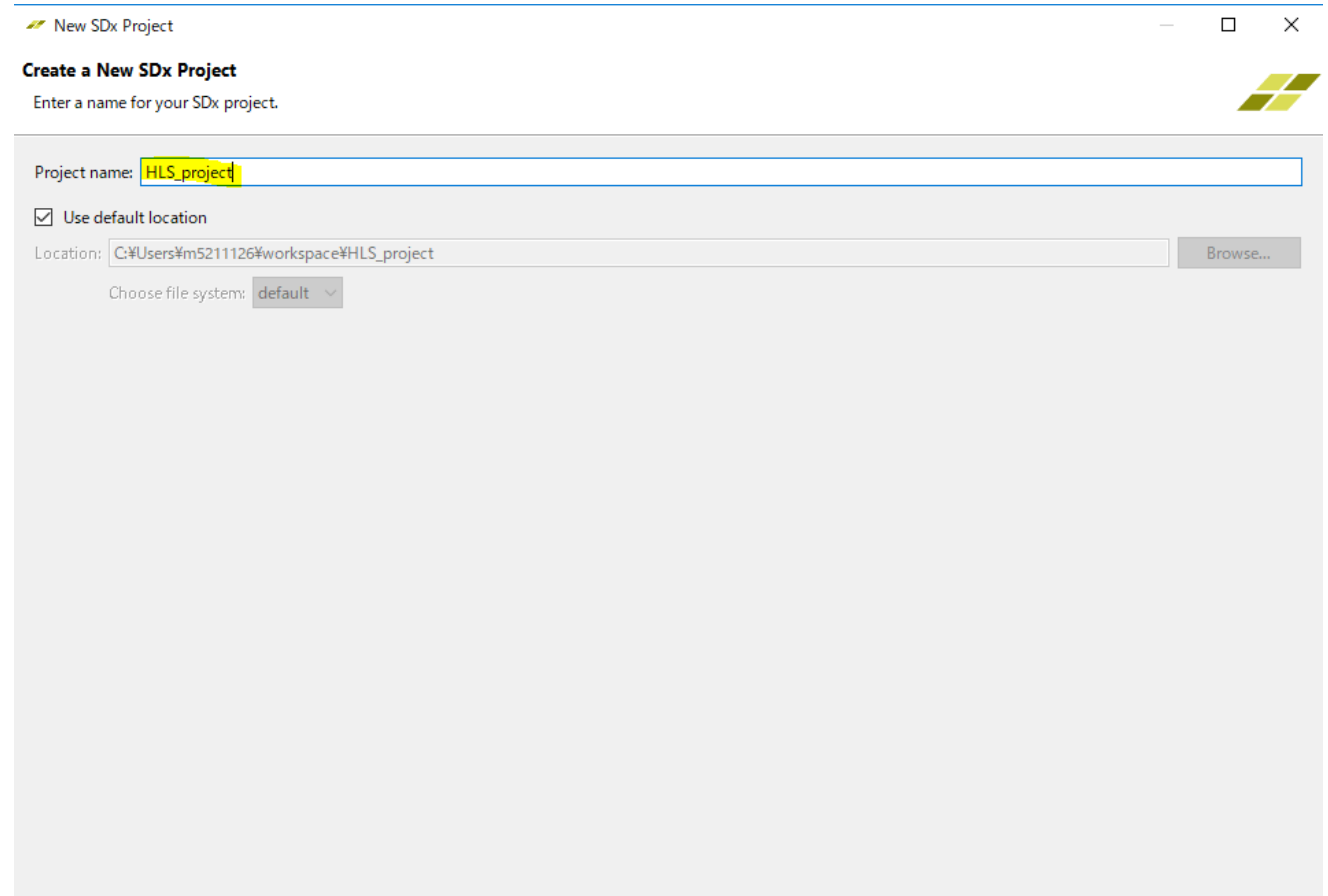
Project type

- Select “Application Project”



Enter project name

- Set “HLS_project”



New SDx Project

Create a New SDx Project

Enter a name for your SDx project.

Project name: HLS_project

Use default location

Location: C:\Users\m5211126\workspace\HLS_project Browse...

Choose file system: default

System configuration

- Set as like the image

New SDx Project

System configuration

Provide the system configuration and software details for your project

Software Platform

System configuration: Linux

Runtime: C/C++

Domain

Domain: linux

CPU: cortex-a9

OS: linux

Additional Settings

Linux Root File System: Browse...

Output type

Executable (elf) Shared Library

Templates

- Unnecessary -> Empty Application

Templates

Select a template to create your project.



Available Templates:

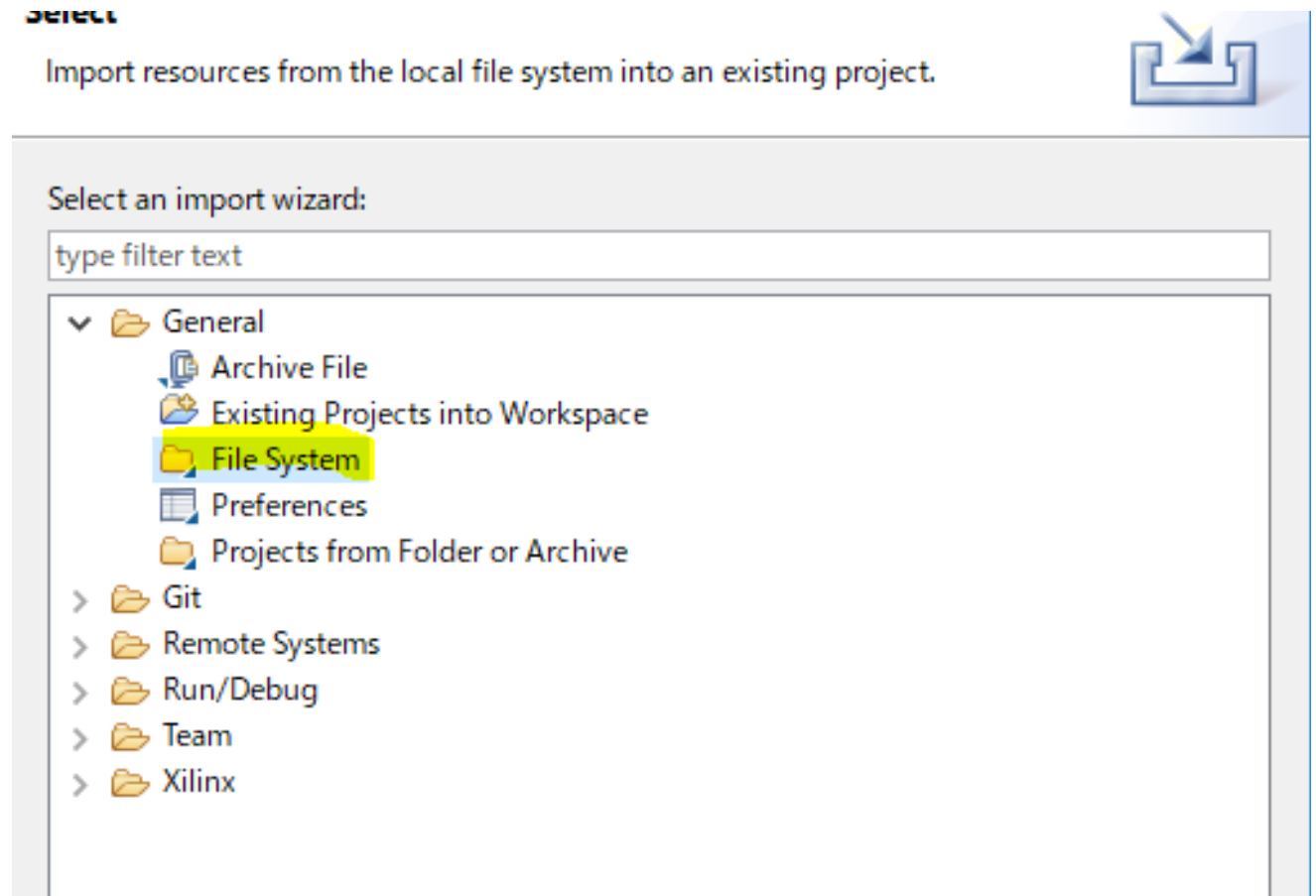
Find: 

Empty Application
▼ hls_lib
Synthesizeable FIR Filter
Array zero_copy ('Short' build time)
Color Space Conversion - RGB/HSV
Emulation Example
Matrix Multiplication and Addition
Matrix Multiplication Data Size

Empty Application
Creates a new Empty application

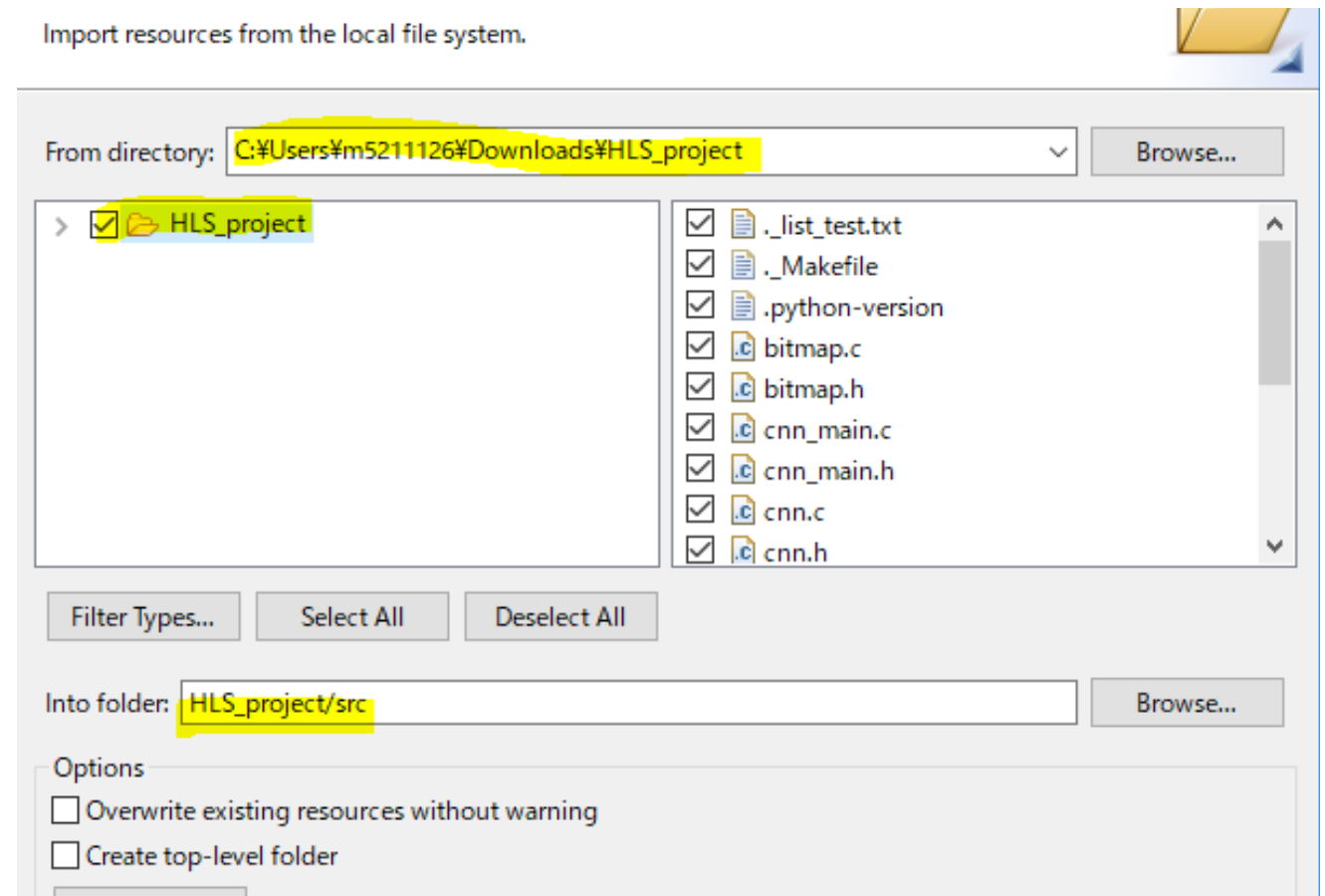
Import files

- Downloads file
“HLS_project.zip”
- Select “File System”



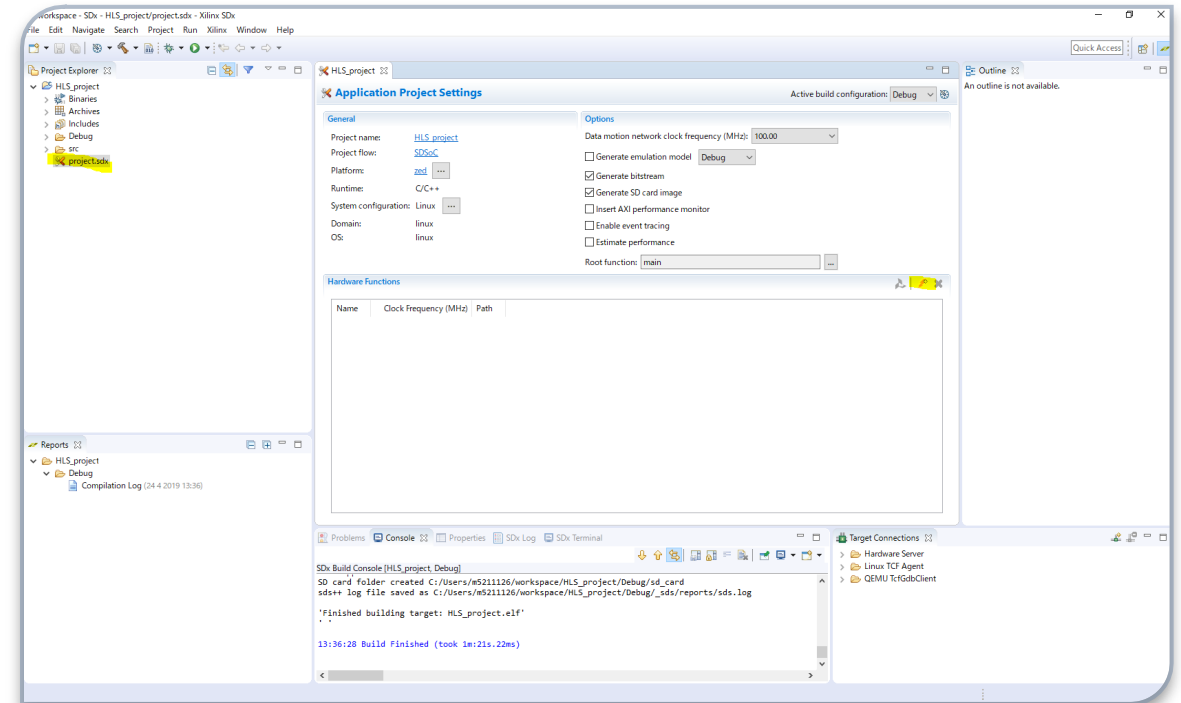
File system

- Select the files
- And “Finish”



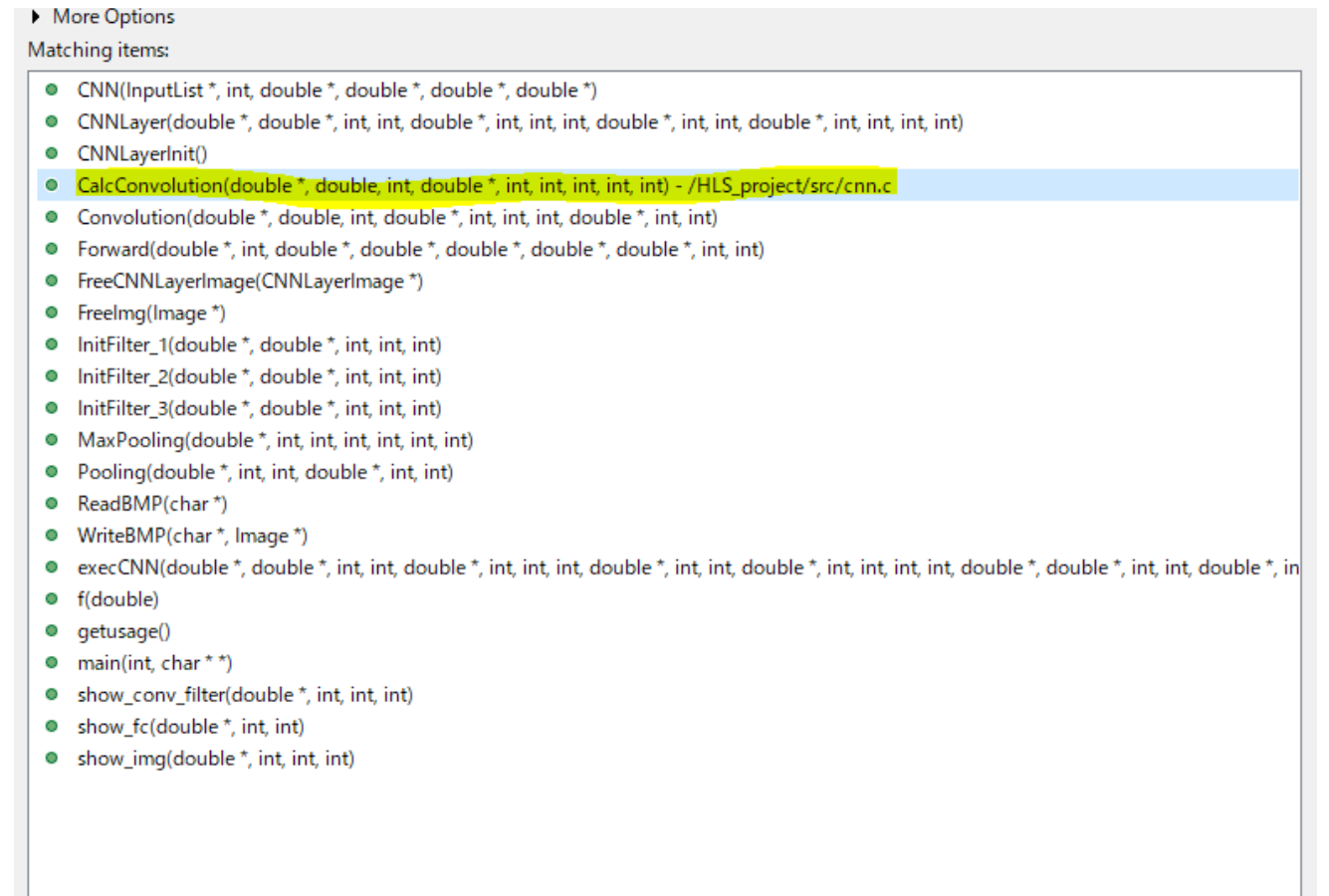
Project window

- “Project Explore” window shows the project files
- Click “project.sdx”
 - See “Application Project Settings”
- Click this mark
 -



Add hardware functions

- Select “CalcConvolution”



Hard ware function is selected

- Now the project should look like this

The screenshot displays the Xilinx IDE interface for an HLS project. The main window is titled "Application Project Settings" with the active build configuration set to "Debug".

General Settings:

- Project name: HLS_project
- Project flow: SDSoc
- Platform: zed
- Runtime: C/C++
- System configuration: Linux
- Domain: linux
- OS: linux

Options:

- Data motion network clock frequency (MHz): 100.00
- Generate emulation model (set to Debug)
- Generate bitstream
- Generate SD card image
- Insert AXI performance monitor
- Enable event tracing
- Estimate performance
- Root function: main

Hardware Functions Table:

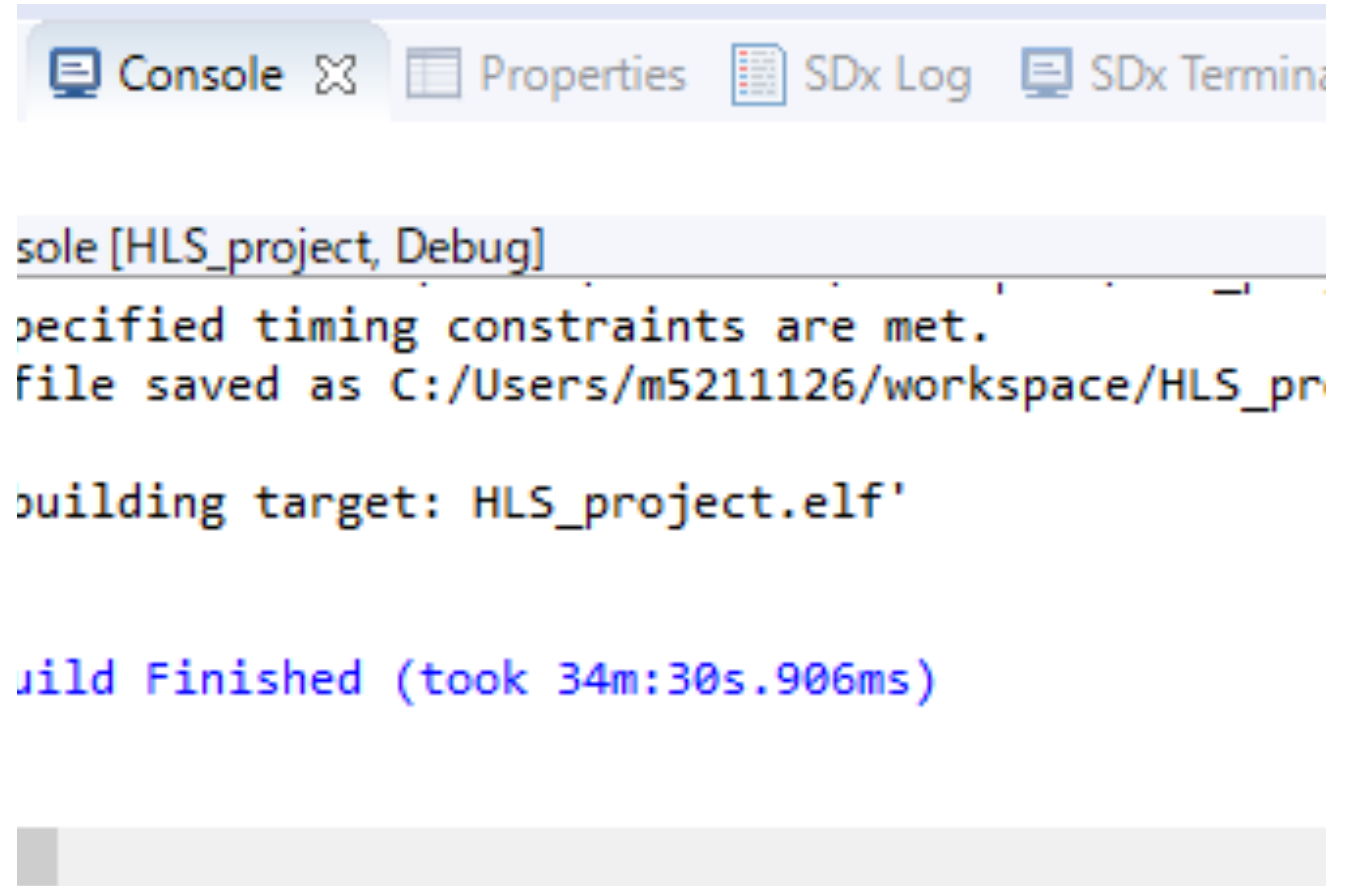
Name	Clock Frequency (MHz)	Path
CalcConvolution	100.00	src/cnn.c

Console Output:

```
SDx Build Console [HLS_project_Debug]
SD card folder created C:/Users/m5211126/workspace/HLS_project/Debug/sd_card
sds++ log file saved as C:/Users/m5211126/workspace/HLS_project/Debug/_sds/reports/sds.log
*Finished building target: HLS_project.eif*
13:36:28 Build Finished (took 1m:21s.22ms)
```


Build project

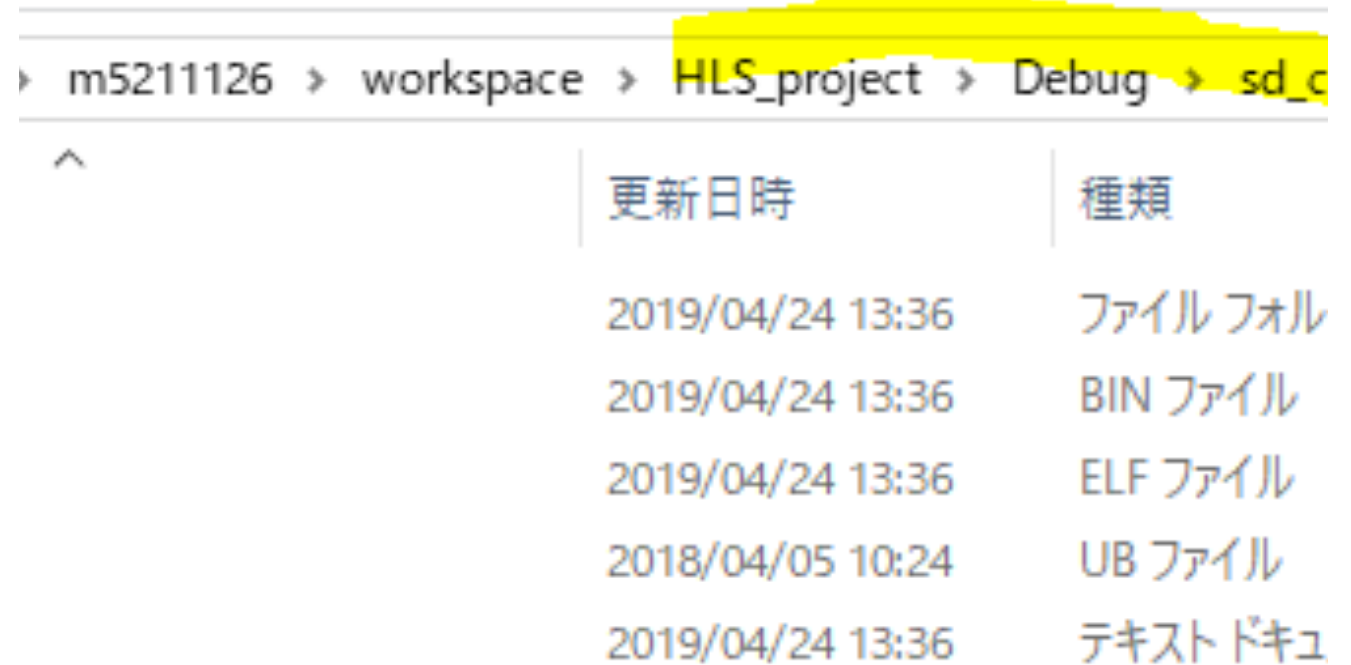
- On “Project Explore” window
 - Right click project folder “HLS_porject”
 - Select “Build Project”
- Build Completion takes about 34 minutes in my case
 - (It depends on machine spec)



```
Console Properties SDx Log SDx Termina  
sole [HLS_project, Debug]  
pecified timing constraints are met.  
file saved as C:/Users/m5211126/workspace/HLS_pr  
building target: HLS_project.elf'  
  
uild Finished (took 34m:30s.906ms)
```

Store the synthesized files to SD card

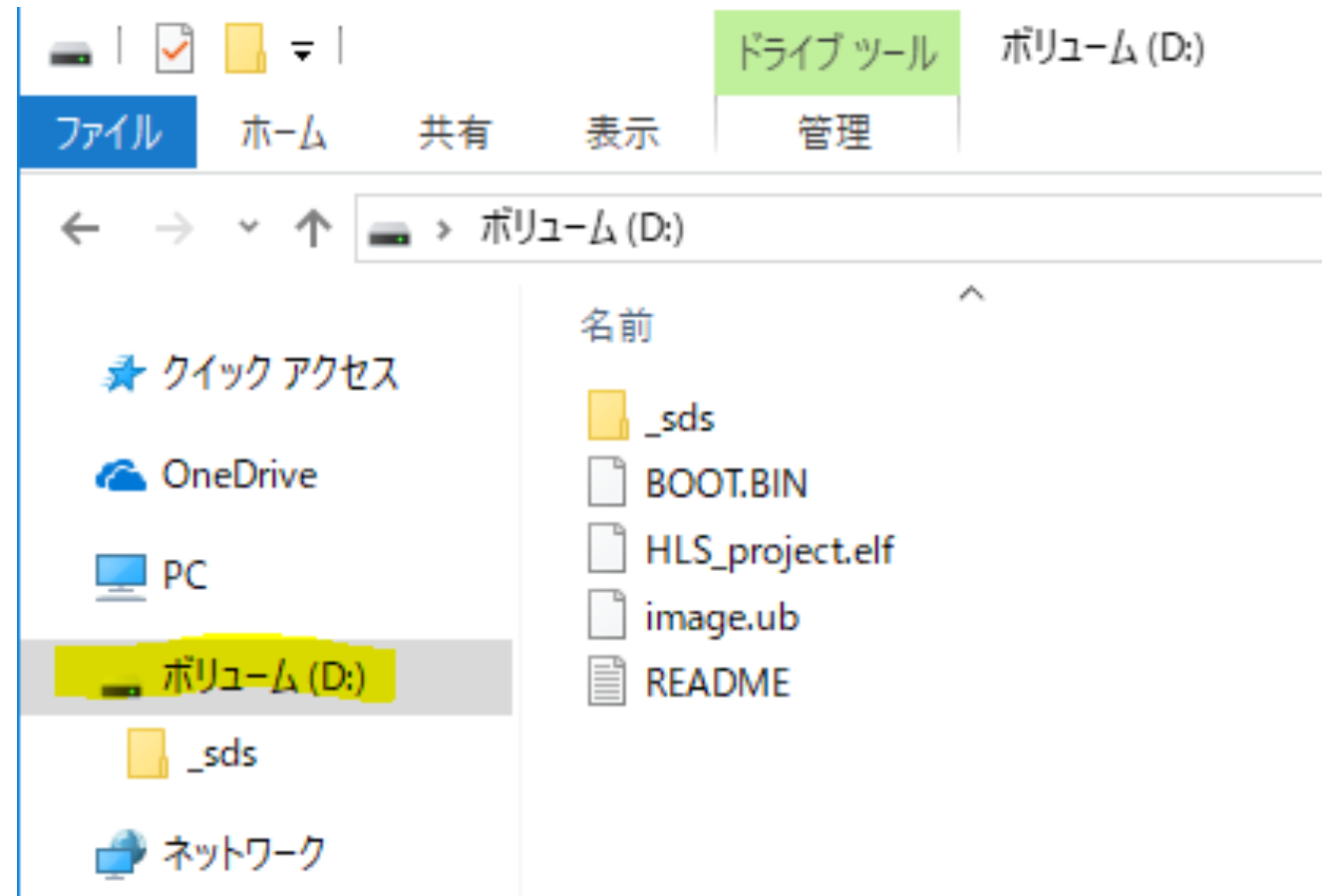
- After the completion of build
- Open the directory
“HLS_project/Debug/sc_card”



更新日時	種類
2019/04/24 13:36	ファイルフォル
2019/04/24 13:36	BIN ファイル
2019/04/24 13:36	ELF ファイル
2018/04/05 10:24	UB ファイル
2019/04/24 13:36	テキストドキュ

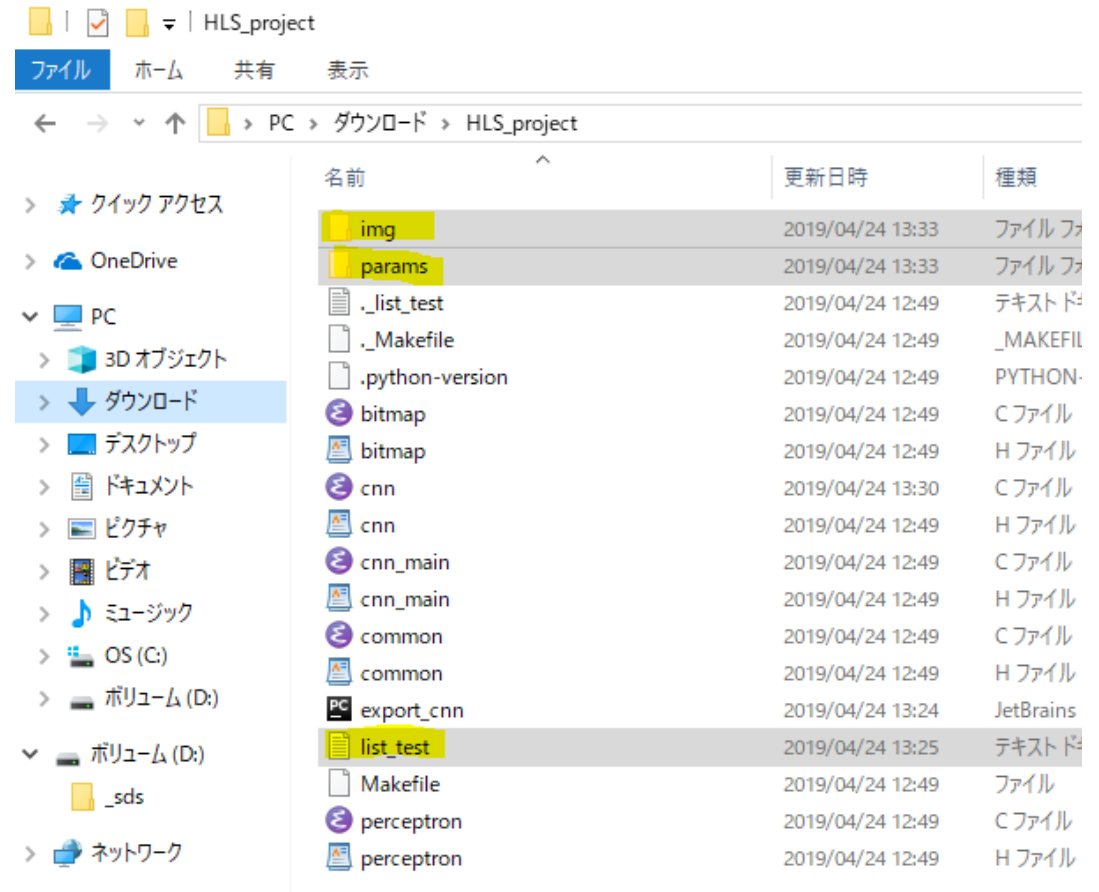
Sd card

- Store the all files in this directory to SD card



Presets files to SD card

- Also add image some files to SD card

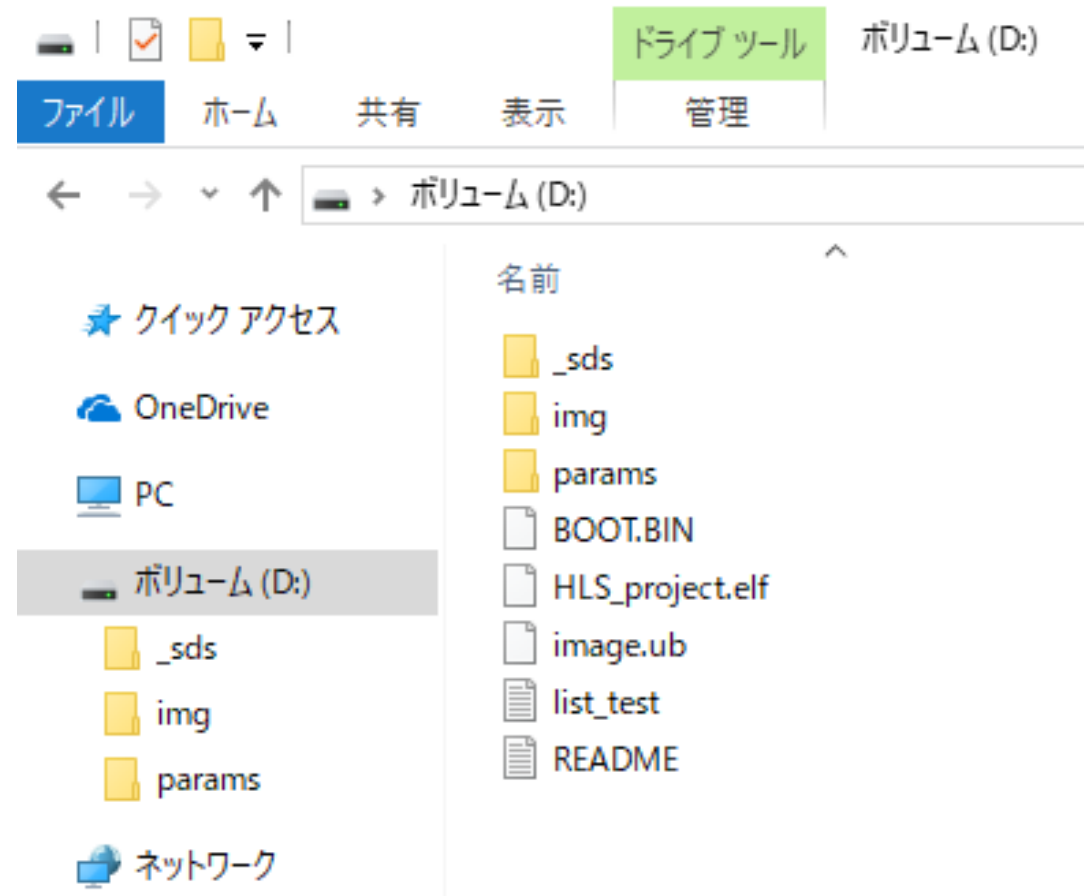


File Explorer window showing the contents of the HLS_project folder. The 'Downloads' folder is selected in the left sidebar. The main pane shows a list of files and folders, including 'img', 'params', and 'list_test', which are highlighted in yellow.

名前	更新日時	種類
img	2019/04/24 13:33	ファイル フォルダ
params	2019/04/24 13:33	ファイル フォルダ
._list_test	2019/04/24 12:49	テキスト ドキュメント
._Makefile	2019/04/24 12:49	_MAKEFILE
._python-version	2019/04/24 12:49	PYTHON-ファイル
bitmap	2019/04/24 12:49	C ファイル
bitmap	2019/04/24 12:49	H ファイル
cnn	2019/04/24 13:30	C ファイル
cnn	2019/04/24 12:49	H ファイル
cnn_main	2019/04/24 12:49	C ファイル
cnn_main	2019/04/24 12:49	H ファイル
common	2019/04/24 12:49	C ファイル
common	2019/04/24 12:49	H ファイル
export_cnn	2019/04/24 13:24	JetBrains
list_test	2019/04/24 13:25	テキスト ドキュメント
Makefile	2019/04/24 12:49	ファイル
perceptron	2019/04/24 12:49	C ファイル
perceptron	2019/04/24 12:49	H ファイル

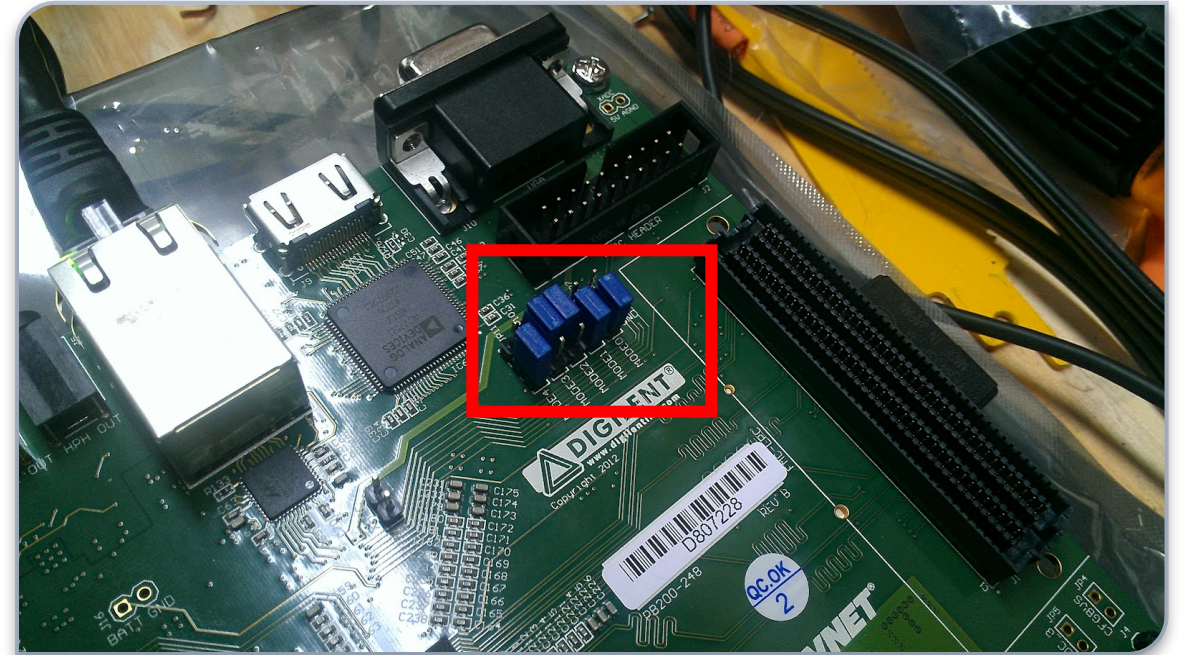
Check SD card

- Files in SD card should be like this



Set SD card into Zed board

- Set the boot mode as “SD boot” on Zed Board.
 - MIO6: GND
 - MIO5: 3V3
 - MIO4: 3V3
 - MIO3: GND
 - MIO2: GND

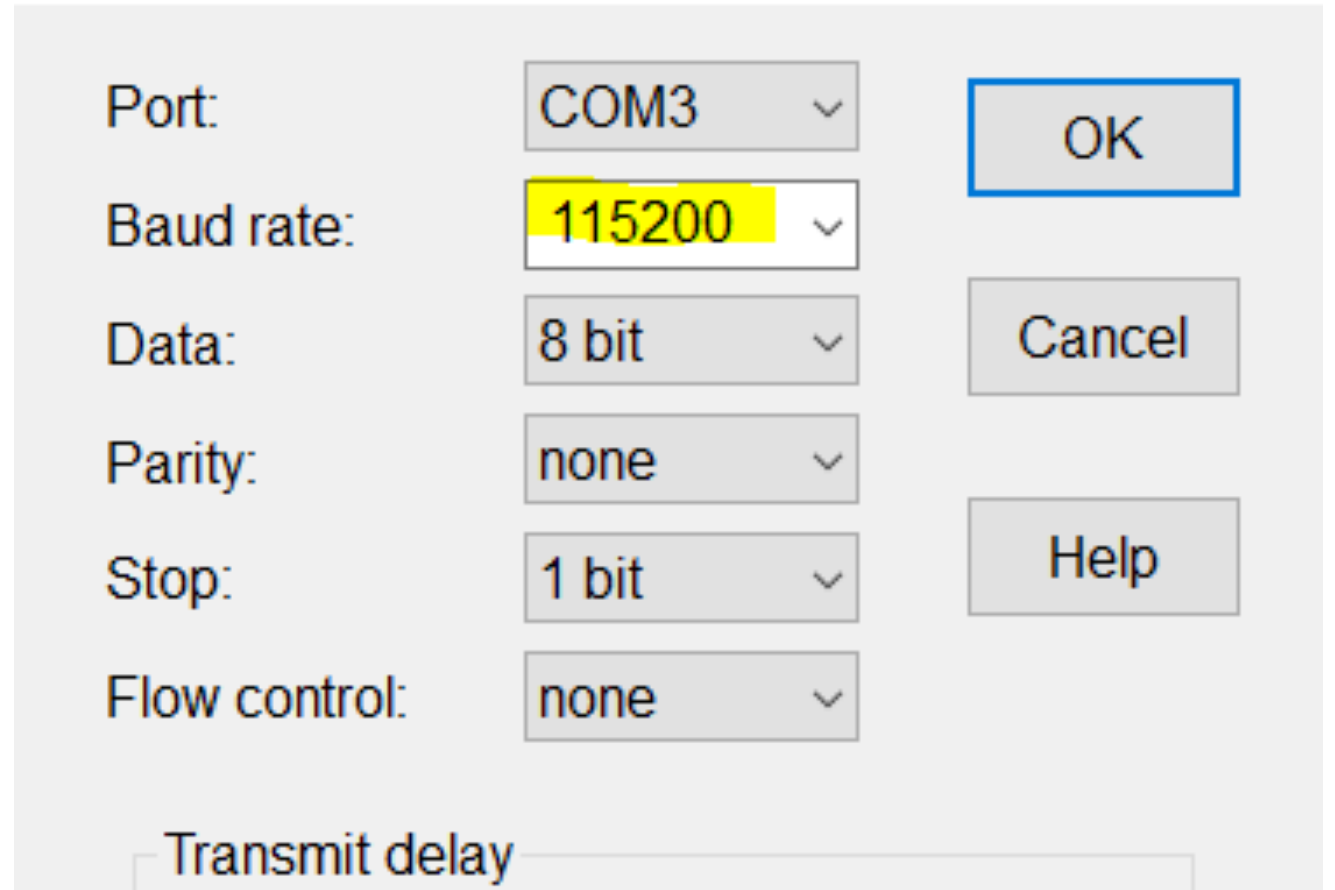


Turn on power on zed board

- Make sure the board is connected with “Prog” and “UART” port with USB connector

Run “tera term vt” for serial communication

- Set as figure



A screenshot of a serial communication configuration dialog box. The dialog has a light gray background and contains several settings, each with a label and a dropdown menu. The settings are: Port: COM3, Baud rate: 115200 (highlighted in yellow), Data: 8 bit, Parity: none, Stop: 1 bit, and Flow control: none. To the right of these settings are four buttons: OK (highlighted with a blue border), Cancel, and Help. At the bottom, there is a label 'Transmit delay' followed by an empty text input field.

Port:	COM3	OK
Baud rate:	115200	Cancel
Data:	8 bit	Help
Parity:	none	
Stop:	1 bit	
Flow control:	none	

Transmit delay

Linux kernel boot

- You can see linux console

```
NET: Registered protocol family 29
can: raw protocol (rev 20170425)
can: broadcast manager protocol (rev 20170425 t)
can: netlink gateway (rev 20170425) max_hops=1
Registering SWP/SWPB emulation handler
hctosys: unable to open rtc device (rtc0)
of_cfs_init
of_cfs_init: OK
ALSA device list:
  No soundcards found.
Freeing unused kernel memory: 1024K
mmc0: new high speed SDHC card at address 0007
mmcblk0: mmc0:0007 DDINC 3.71 GiB
INIT: mmcblk0: p1
version 2.88 booting
Starting udev
udevd[765]: starting version 3.2.2
udevd[766]: starting eudev-3.2.2
hwclock: can't open '/dev/misc/rtc': No such file or directory
Mon Mar 19 21:56:25 UTC 2018
hwclock: can't open '/dev/misc/rtc': No such file or directory
Starting internet superserver: inetd.
Configuring packages on first boot....
(This may take several minutes. Please do not power off the machine.)
Running postinst /etc/rpm-postinsts/100-sysvinit-inittab...
Running postinst /etc/rpm-postinsts/101-mnt-sd...
```

Move to SD card partition

```
root@zed:~# cd /mnt/  
root@zed:/mnt# ls  
BOOT.BIN          System Volume Information  img  
HLS_project.elf  _sds                      list_test.txt  
README.txt       image.ub                  params  
root@zed:/mnt#
```

Run application

- Run “./HLS_project.elf”
- This time the hardware function is applied no optimization
- Test classification
 - Classify 10 images
 - 0: Cat
 - 1: Dog
- It took 1832.814 ms for classify each picture

```
root@zed:/mnt# ./HLS_project.elf
CNN - Start
Mode: Test
List File: list_test.txt
Num of Input Data: 10
File: /mnt/img/000.bmp(0)
[Answer] -0.664498
File: /mnt/img/001.bmp(0)
[Answer] 0.272151
File: /mnt/img/002.bmp(0)
[Answer] -0.948464
File: /mnt/img/003.bmp(0)
[Answer] -0.159920
File: /mnt/img/004.bmp(0)
[Answer] -0.216047
File: /mnt/img/005.bmp(1)
[Answer] 0.462996
File: /mnt/img/006.bmp(1)
[Answer] 0.362923
File: /mnt/img/007.bmp(1)
[Answer] 0.387195
File: /mnt/img/008.bmp(1)
[Answer] -0.109920
File: /mnt/img/009.bmp(1)
[Answer] 0.411720
UsageTime: 1832.814[ms]
root@zed:/mnt#
```

Shutdown

- Type
 - Shutdown `-h now`
- System halted
 - You can power off Zed Board

```
zed:/mnt# shutdown -h now

Last message from root@zed (ttyPS0) (Mon Mar 19 22:04:41 2018):

System is going down NOW!
Sending processes the TERM signal
zed:/mnt# Stopping Dropbear SSH server: stopped /usr/sbin/dropbear (r
ar.
k: can't open '/dev/misc/rtc': No such file or directory
ng syslogd/klogd: stopped syslogd (pid 1239)
d klogd (pid 1242)

ng tcf-agent: OK
iguring network interfaces... done.
g all processes the TERM signal...
g all processes the KILL signal...
ting remote filesystems...
vating swap...
ting local filesystems...
: System halted
```

Summary

- How to use SDx IDE 2018.1 for HLS was demonstrated
- CNN circuit was designed