Adaptive Systems Laboratory Research Introduction

Adaptive Systems Laboratory, Division of Computer Engineering
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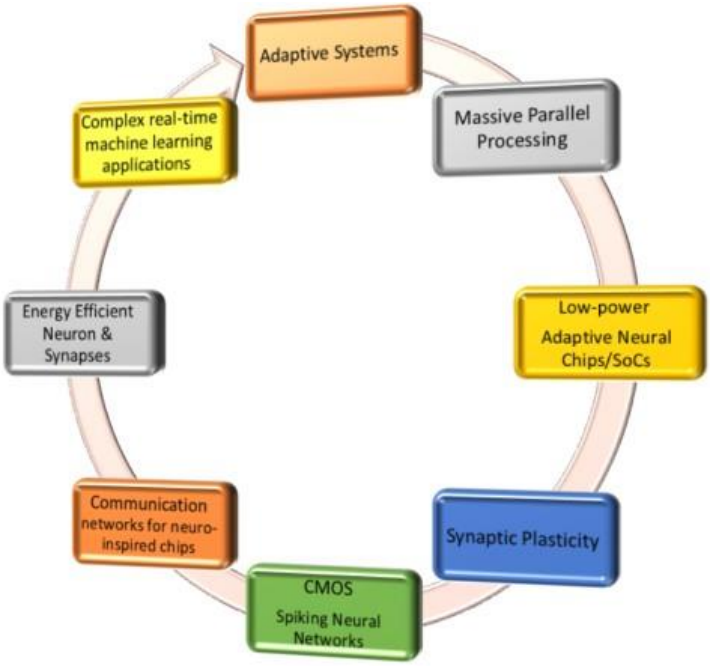
ASL focuses on energy-efficient adaptive computing systems based on neuronal algorithms and fault-tolerant scalable interconnects to overcome the limitation of traditional stored-program computing style. In particular, we are investigating the computational properties of neural processing systems by developing new chips and systems that emulate the principles of computation in the neural systems. Our applications range from neuro-inspired (brain-like) low-power computing embedded systems to adaptive neural-based control, and brain-machine interfaces.



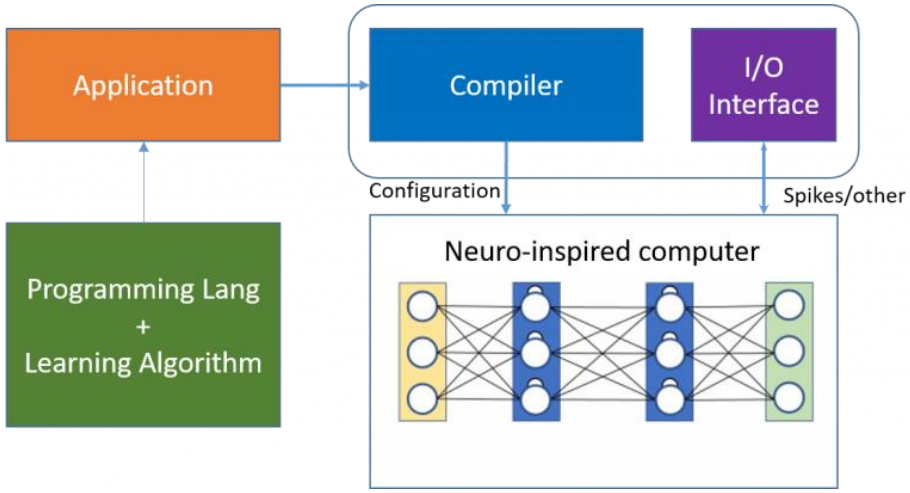
Currently, we are investigating the following two main related research areas:

Adaptive Neuro-inspired Computing Systems and Platforms

The biological brain implements parallel computations using a complex structure that is different from the conventional stored-program computing style. Our brain is a low-power, fault-tolerant, and high-performance machine! It consumes only about 20W and brain circuits continue to operate as the organism needs even when the circuit (neuron, neuroglia, etc.) is perturbed or died.
Computations in neural networks are naturally parallel and distributed among billion neurons. This very high degree of distributed parallelism with the continuous advances in

neuro-inspired engineering and neuroinformatics will enable the development and manufacture of low-clock frequency (low-power) and high-throughput neuro-inspired computing architectures and systems.

Hardware implementations of neural networks are very efficient and effective methods to provide cognitive functions on a chip compared with conventional stored-program computers/processors. One of the most difficult of the challenges in modeling the brain is the massive interconnectivity. So, the challenges that need to be solved include building a small-size massively parallel architecture with scalable interconnects, low-power consumption, and reliable circuits.



Our focus is to investigate novel neuro-inspired computing systems and adaptive low-power neural chips/SoCs able to scale up to biological levels. Currently, we are studying the following topics:

- Neuro-inspired neural network models and computing methods
- Low-power adaptive neural chips
- Spiking neural architecture building blocks
- Conventional hardware (i.e. VLSI, FPGAs) and innovative hardware (i.e., memristor) implementation of Neuro-inspired systems
- Synaptic and structural plasticity circuit emulations
- Reliable and scalable communication networks for neuro-inspired chips/systems;
- Neural circuits, models for neurons and synapses
- Ultra-low power biological-scale neurons
- Reconfigurability and adaptability methods
- On-chip learning algorithms

Energy-efficient Fault-tolerant Scalable Interconnects

Future computing systems would contain hundreds of components made of processor cores, DSPs, memory, accelerators, and I/O all integrated into a single die area of just a few square millimeters. Such ”tiny” complex system would be interconnected via a novel on-chip

interconnect closer to a sophisticated network than to current bus-based solutions. This network must provide high throughput, low latency, and also fault-tolerance while keeping area and power consumption low. Three-dimensional Networks-on-Chip (3D-NoC) is an auspicious solution to alleviate the interconnect bottleneck and reduce the power consumption in current System-on-Chips (SoCs) designs. However, 3D-NoC systems are becoming susceptible to a variety of faults caused by crosstalk, the impact of radiations, oxide breakdown, and so on. As a result, a simple failure in a single transistor caused by one of these factors may compromise the entire system reliability where the failure can be illustrated in corrupted message delivery, time requirement unsatisfactory, or even sometimes the whole system collapse.

Our research effort in this area is about solving several design challenges to enable the packet-switched and other novel switching schemes for networks of massively parallel cores in conventional load/store and in a novel neuro-inspired computing systems. We are currently investigating the following topics: Low-power interconnects for an event-driven large network of neuromorphic cores; Implementation techniques for TSV based NoCs; 3D-IC integration; Fault-tolerant and reliability issues; New topologies and flow-control methods; Photonic Interconnects; Organic circuits.

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