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NASH Project

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Abstract

The biological brain implements massively parallel computations using a complex architecture that is different from current Von Neumann machine. The brain is a low-power, fault-tolerant and high-performance machine! It consumes only about 20W and brain circuits continue to operate as the organism needs even when the circuit (neuron, neuroglia, and so forth) is perturbed or died. Our goal in this project is to research and develop an adaptive neuro-inspired system-on-chip and platform (NASH) with on-chip learning and cognitive capabilities targeted for pattern recognition and complex cognitive tasks. This article descibes in a fair amount of the detaiuls the NASH system architecture.

1. Introduction

Current neural processing methods are based on a so-called spiking neural networks (SNNs), which differ from conventional artificial NN models, where information is transmitted using spikes or pulses (see Fig. 1).
Brain-inspired models, such as SNNs, offer the opportunity to design a resilient system for performing computation with low power. SNNs offer the potential to mimic the ability of the brain to tolerate faults and repair itself [1]. The brain often replaces neurons by reconnecting to newly generated neurons via synaptic junctions. This adaptability allows the brain to overcome faults.

Software simulation of traditional SNN networks face the problem of scalability in that biological computing systems are inherently parallel in their architecture whereas conventional systems are based on sequential processing architectures. Whereas, hardware SNNs have the advantage of computational speed over software simulations and can take full advantage of their inherent parallelism. In particular, hardware SNNs can respond to the demands of real-time and fault-tolerant applications. However, the current problem of interneuron connectivity is prohibiting the implementation of efficient hardware of these SNNs. This connectivity issue is more challenging when neuro-glia networks are also considered.

One promising approach to this challenge connectivity is the use of packet-switched Network-on-Chip (NoC) to support the fast exchange of information within an SNN.

Our goal is to develop dedicated mixed signals programmable Neural-Network architecture which will support the implementation of large-scale SNN applications.

Current FPGAs do not provide sufficient dedicated programmable hardware resources (i.e. synaptic junctions, inline training support) which needed for efficient SNN implementations. Also, FPGAs routing structures cannot accommodate the high levels of interconnection found in SNNs.

The proposed NASH architecture avoids these problems by making use of small-scale low-powered analog spiking neuron cells as the central PE. Combining small size low power neuron cells with the OASIS-NoC routing capability will lead to NASH system that can significantly increase the processing power of SNNs towards the biological scale. However, the use of the OASIS-NoC as an interconnection fabric for large scale neuro-glia networks demands a more challenging trade-off between power consumption, throughput and network scalability, and therefore an improved solution is required. Scaling is one of the key issues associated with all complex electronic systems because interconnect consumes large areas of chip real-estate and subsequently causes longer critical path delays [1].

To solve the large scale implementation issues of reconfigurability and programmability, lightweight synapse weight storage and interneuron connectivity, a new efficient architecture is required.

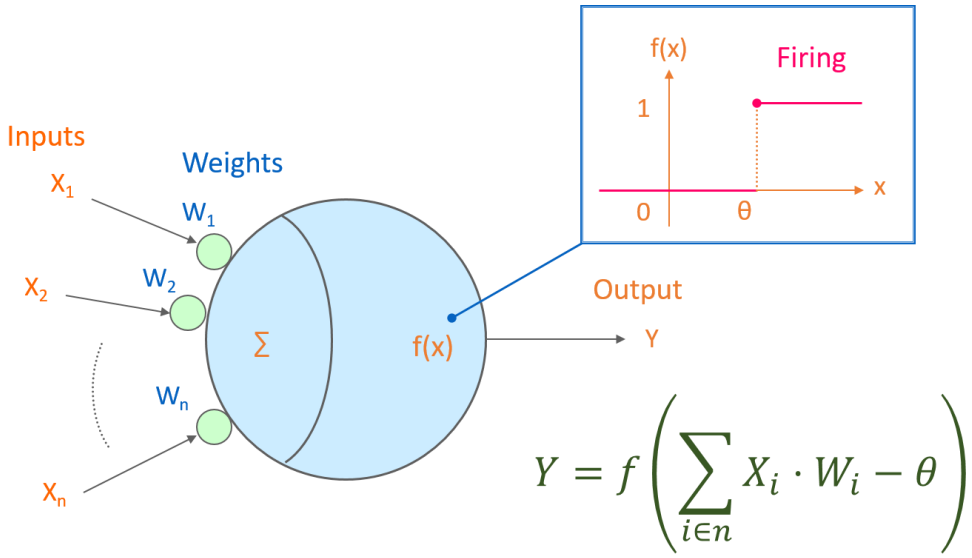
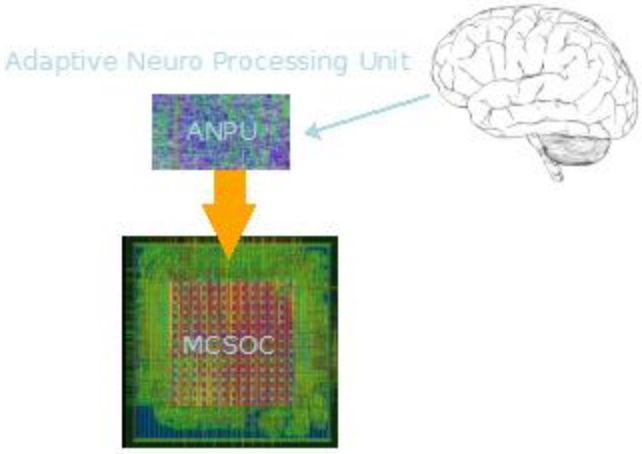


Fig. 1. Neuron Model (McCulloch-Pitts Model of Neuron). W1, W2,…Wn are weight values normalized in the range of either (0,1) or (-1,1 and associated with each input line.

To demonstrate the NASH implementation of an SNN, an FPGA hardware implementation will be developed and interfaced to a drone or a robot. This project is based on an existing scalable OASIS-NoC routers developed at ASL [2-21] and explored the following issues in the development of a new NoC strategy for SNN:
(1) An efficient topology and configurations which enable reconfiguration of different NoC networks in hardware;
(2) A mixture of different basic NoC topologies (OASIS-2D, OASIS-3D, and so forth) will be investigated;
(3) Performance evaluation and comparisons against existing systems.



NASH High-Level View

2. Hardware SNN Architectures

A major challenge in developing SNNs in hardware is the development of neuro-inspired platforms which can support scalable low-power realizations and reprogrammable interconnect. In particular, the problem of interneuron connectivity is the major problem that prohibits the implementation of such SNNs.

Current attempts to realize SNNs using multiprocessors in hardware have included limited numbers of neurons due to connectivity issues [22-27].
Several full-custom neuromorphic architecture devices have been proposed [28-30] which aim to address the inefficiencies of FPGAs by including optimized synaptic cells and Address Event Representation (AER) routing [33]. However, these systems are not reconfigurable and cannot scale due to limited connectivity provided by AER between neurons.

3. NASH Architecture

NASH combines the programmability features of FPGAs and the scalable interconnectivity of OASIS NoC with low-area and low-power spiking neuron cells with training and learning capability. The proposed system uses individual routers to group *n* synapses and the associated neuron via a macroblock named neuro-title (NT).

The functionality and the connectivity of each NT in NASH system can be programmed to realize neuron-level functions. NASH configuration data is propagated from source PE to destination PE via time-multiplexing using the NoC routing modules. During runtime, spike events occurring in layer one are forwarded to the associated synapses of layer 2 via several routerss.

The idea of the macroblock title is in the merging of analogue synapse/neuron circuitry with NoC digital interconnect to provide a scalable and reconfigurable neural building block. Other schemes, such as in [26,27], are also based on NoC routers but with software models of synapse and neurons running on microprocessors.

3.1 Spike communications

OASIS NoC router controls the inputs and outputs of the cells (neurons). The event of a given spike is received in the form of a data packet as shown in Fig. 3.

Each time a spike event occurs within the NT, the tile routers send an output packet. The proposed scheme of connecting neural tiles allows various SNN topologies, such as recurrent networks and multilayered feed-forward, to be implemented.

3.2 Neuro-Tile Architecture

TBC

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